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A Novel Inductively Degenerated CMOS LNA for UWB Applications

Jaya Anand[1], Nutan Lata[2] and Vijay Nath[3]

[1]Department of Computer Engineering, University of California, San Diego, USA
[2]Department of Physics, Doranda College, Ranchi University, Ranchi, India
[3]Department of Electronics and Communication Engineering, BIT Mesra, India

ABSTRACT

This paper demonstrates the inductively source- degenerated CMOS LNA designed for UWB applications. LNA is the building block of a RF receiver. The newly designed CMOS LNA utilizes the 180nm technology which provides a gain of 11 dB, with a noise figure of 3 dB over the entire range of operation.

KEYWORDS
Cascade; CMOS; Chebyshev;
Common Source;
Low Noise Amplifier (LNA);
Noise Figure (NF);
Source Follower;
Ultra-Wide Band (UWB)

1. INTRODUCTION

There has been a recent boom in wireless consumer applications, which has emphasized the need for low-cost, highly integrated RF parts. A steady improvement in transistor performance and the desire for higher level of integration have led to an increase in the application of silicon technology. While power consumption is gradually increasing and hence becoming a controlling factor in the CMOS receiver design, the development of low power RF circuit techniques requires our sincere attention. The first on-chip active stage of an RF receiver is usually a low-noise amplifier (LNA). The Friis equation, which is already well known, puts forward two of its most important specifications- low noise factor and high gain [1].

LNA is key building block of RF receiver of wireless communication. It is used to amplify weak signals from an antenna at low noise levels. As LNA is the first block of the entire receiver system, it should be designed with low noise figure so that the noise figure of the overall system is low. LNA is used in numerous applications like radio astronomy application, wireless local area networks, telecommunications, radar systems and satellite communications etc. Basic features of LNA include gain, noise figure and input and output return losses (IRL, ORL). All these features of the LNA are represented by S parameters of the amplifier. Moreover, some other important features to be considered while designing a LNA include linearity, dynamic range, bandwidth, stability and power dissipations.

LNA circuits are generally designed as Common Source (CS) or Common Gate (CG) stages. Proper LNA circuit design is chosen based on the application for which the LNA is designed and the designer applications. For each application, some LNA characteristics are more important than the others and this forms the basis for the designer to choose proper circuit for LNA.

The basic Common Source LNA (CS-LNA) topology provides better noise performance than the Common Gate LNA (CG-LNA) topology at low operating frequencies relative to the MOSFET fT; however, lower noise figure can be achieved by using off-chip matching components or high-power consumption. Hence, the CS-LNA topology is sub-optimum in low power fully integrated applications.

This paper presents an inductively degenerated CMOS LNA for UWB applications. A UWB signal is defined as a signal with a bandwidth higher than 20% of its center frequency, or a signal with a bandwidth higher than 0.5 GHz. The American Federal Communications Commission (FCC) specified a band of operation for UWB signals from 3.1 to 10.6 GHz. It is divided into V sub-sections. Section II gives the different LNA topologies, Section III gives the proposed LNA design, Section IV gives the Simulation Results and Section V gives the Conclusion.

2. DIFFERENT LNA TOPOLOGIES

Various topologies of designing a LNA are classified as:

1. CS topology
2. CS with source degenerated with inductor topology
3. Self-bias CS/inductive degeneration topology
4. Current reuse common gate topology
5. Distributed LNA topology
6. Resistive feedback topology
7. Cascode LNA topology

The above-mentioned design topologies can be briefly described as follows:

1. The basic common source (CS) topology [1, 2] has low noise figure but moderate gain compared to the other topologies
2. The CS topology with source degenerated inductor [3, 4] has a good trade-off between noise figure and gain.
3. The self-bias topology [5,6] avoids the application of bias at the gate of the CMOS.
4. The current reuse common-gate topology [7] has the same current flowing through the two CMOS with both gates of the CMOS grounded.
5. The distributed topology [8] has all the gates connected at one point and all drains connected to some other point which leads to the ultra-wide bandwidth.
6. The resistive feedback topology [9] has a resistor between the gate and drain such that it compensates the effect of Cgd and offers better noise figure and gain compared to the other topologies but offers high noise figure at low frequency band.
7. The cascode LNA offers high power gain, good noise performance, lower power consumption and high reverse isolation. At lower microwave frequencies [10], the noise sources of the upper transistors of cascode stage are degenerated by the lower transistor output impedance, which offers superior noise performance, with the degradation of this performance at higher frequencies.

Table 1: Comparison between various LNA topologies

Topology	Advantage	Disadvantage
Resistive termination	Good input match	Large NF
Common gate	Excellent input match	Large NF and power
Series shunt feedback	Broadband I/O match	Stability issues
Inductive degeneration	Good narrowband match, Small NF	Large area
Current reuse	High gain low power	External matching network required
Inductor neutralization	Good reverse isolation (S22)	Increased area, stability concerns

3. PROPOSED CMOS LNA

The proposed LNA is shown in Figure 1. Resonance in the reactive part of the input impedance can be achieved using a Chebyshev filter in the frequency range from 3 GHz to 10 GHz. Typically, a Chebyshev filter consists of two capacitors and two inductors. It works as a pass-band filter, if the values of the inductors and capacitors are chosen correctly.

The overall reactance can be resonated over a wider bandwidth with the help of inductively generated common source transistor. The inductor placed in series with the capacitor adds flexibility to the design on the input side. The cascade connection of MOS transistors improves the reverse isolation and frequency response. The source follower stage is used for measurement purposes.

At high frequencies, MOS transistors act as current amplifiers, due to Channel Length Modulation effects.

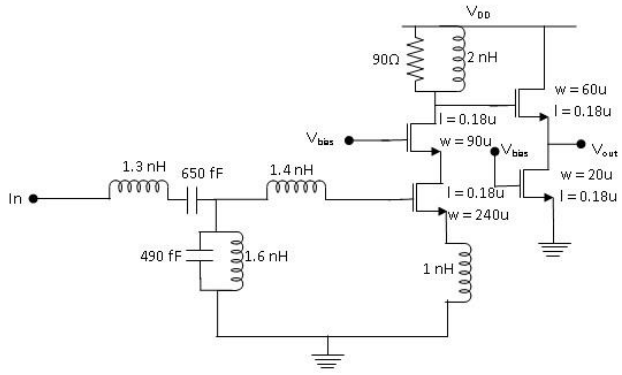

Fig. 1 Schematic of the Proposed CMOS LNA

4. SIMULATION RESULTS

The proposed circuit is simulated using Cadence 180 nm CMOS technology. The simulation results are presented in Table 2 shown below. The proposed LNA has a gain of 11dB and Noise Figure less than 3dB for the entire range of operation ranging from 3GHz to 10GHz.

Frequency (in GHz)	Gain (in dB)	Noise Figure (magnitude)
4	10.2	1.95
6	11	2.1
8	10.6	2.87
10	10.04	2.6
12	9.98	2.5
14	11.2	2.7

Table 2: Simulation results for the proposed LNA

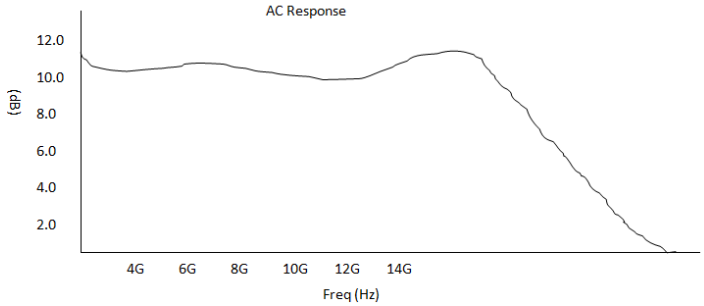

Fig. 2 Gain vs Frequency Simulation for the Proposed LNA

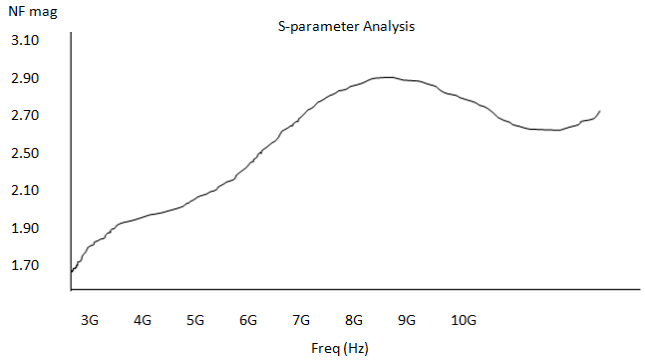

Fig. 3 Noise Figure Simulation for the Proposed LNA

5. CONCLUSION

The proposed circuit shows the CMOS LNA which can be used for UWB applications. The LNA is intended to provide enough gain in the frequency range from 3GHz to 14GHz. CMOS 180nm technology is used in the proposed design. The proposed design has a gain of 11 dB and noise figure is below 3 dB for the entire range of operation.

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AUTHORS

Jaya Anand received her B.Tech degree in Electronics and Communication Engineering from BIT Mesra, India in 2019 and MS degree in Computer Engineering from University of California, San Diego, United States of America in 2023. She has previously worked in Synopsys, Bengaluru as an AMS Circuit Design Engineer, and interned at Apple, California as Custom Circuit Design Engineer.

Email: jaya.anand2k10@gmail.com

Nutan Lata received here MSc degree in Physics with Electronics as her special paper from Bihar University, Muzaffarpur. She obtained her PhD degree in Electronics from Ranchi University, Ranchi, on the topic **‘An investigation into current conveyor based sinusoidal oscillator circuits’.** She is working as an Assistant Professor in the Department of Physics, Doranda College, Ranchi, under Ranchi University, Ranchi, since 2009. She has authored and co-authored several books for undergraduate classes. She has also published several papers in referred journals and has participated in several conferences.

Email: drnutanlata@gmail.com

Vijay Nath received his BSc degree in physics from DDU University Gorakhpur, India in 1998 and PG Diploma in computer networking from MMM University of Technology Gorakhpur, India in 1999 and MSc degree in electronics from DDU University Gorakhpur, India in 2001, and PhD degree in electronics from Dr. Ram Manohar Lohiya Avadh University Ayodhya (UP) and in association with CEERI Pilani (Raj), India in 2008. His areas of interest are ultra-low-power temperature sensors for missile applications, microelectronics engineering, embedded system design, cardiac pacemaker, IoT, AI/ML.
Corresponding author Email: profvnath@gmail.com