ISSN: 2584-0495 Vol. 3, Issue 1, pp. 1480-1486

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

A 406.08pW CMOS Temperature Sensor with Sensing Range of -20℃ to 100℃

Rahul Kumar Raj, Nikhat Anjum, and Vijay Nath

Cite as: Rahul Kumar, R., Anjum, N., & Nath, V. (2025). A 406.08pW CMOS Temperature Sensor with Sensing Range of -20℃ to 100℃. International Journal of Microsystems and IoT, 3(1), 1480–1486. https://doi.org/10.5281/zenodo.15471848

Published online: 20 January 2025

DOI: . https://doi.org/10.5281/zenodo.15471848

International Journal of Microsystems and IoT
Vol.3, Issue 1, pp.1480-1486; DOI: https://doi.org/10.5281/zenodo.15471848

Check for updates

A 406.08pW CMOS Temperature Sensor with Sensing Range of -20℃ to 100℃

Rahul Kumar Raj, Nikhat Anjum, and Vijay Nath

Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, India

ABSTRACT

This proposed article introduces a design for a low-energy temperature sensor that removes the need for bipolar junction transistors (BJTs). As an alternative, the sensor leverages the temperature dependence of MOSFETs' threshold voltage, simplifying the circuit layout and decreasing power consumption. The proposed sensor structure uses five transistors running inside the subthreshold region, ensuring ultra-low energy operation. The design has been extensively simulated and demonstrated using the Cadence simulation environment with the gpdk 90nm CMOS generation library. The circuit operates with an ultra-low supply voltage of ±0.1V, making it especially suitable for low-strength applications. The sensor is specially optimized for on-chip thermal sensing inside a temperature variety of -20°C to +100°C, protecting a broad spectrum of operating situations. one of the key features of this design is its remarkably low power intake, that is measured to be only 406.08 pW, and only inaccuracy of ±0.1°C, making it a remarkable desire for strength-restrained environments consisting of wearable electronics, implantable medical devices, and IoT sensors. The simplicity of the layout, blended with its electricity performance, underscores its potential for integration into cutting-edge low-electricity ICs, wherein thermal monitoring is essential for overall performance optimization and reliability assurance.

KEYWORDS

CMOS Temperature Sensor; Smart Sensor; Low Power; Pico Watt; weak Inversion Region; Thermal management; IoT

I. INTRODUCTION

Smart temperature sensors that are fully integrated and cost-effective are widely used in many different applications, including office or home electronics, automotive systems, and thermal management in portable consumer electronics. They are also necessary for many safeties systems' heat detection [1]. The temperature could be a very essential physical quantity in our daily life. It is implemented in various fields, including clinical, space, semiconductor, wearable devices, biomedical, and automobile industries etc. In semiconductor devices, temperature tracking plays an essential role in preventing heating issues and thermal management of devices. Nowadays, it's a heavy call. The use of CMOS-based temperature sensors is advantageous for thermal management, as they help in accurately tracking device heat [2].

Numerous CMOS temperature sensors with varying temperature ranges and accuracy levels have been suggested and constructed. When designing temperature sensors with CMOS technology, one of three main approaches is typically used: bipolar junction transistor (BJT), threshold voltage, or inverter delay [3]. Most CMOS temperature sensors have different accuracies and temperature ranges in their designs. Because of the limitations of MOSFET operating characteristics, the range of operating temperature is usually restricted to 20°C to 130°C. Because of their greater precision, BJT-based CMOS temperature sensors are especially well-liked among these sensors. These sensors depend on the forward-bias base-emitter junction of the BJT's CTAT or PTAT behavior. But as CMOS process technology advances, BJT performance declines, frequently necessitating external curvature correction.

Furthermore, the idea of inverter delay, which is also temperature-dependent, has served as the foundation for the development of numerous CMOS temperature sensors. One benefit of this design technique is that it is entirely digital. However, it needs a clock signal that is independent of temperature, which poses a serious challenge for implementation [4]. Since its creation, the suggested temperature sensor has experienced substantial advancements. With a power consumption of only 406.08pW, it was made to function in the temperature range of -20°C to

100°C [5,6,7].

Recent developments in CMOS temperature sensors have placed a high priority on improving the sensors' overall performance, paying particular attention to crucial elements including durability, linearity, and precision. Considerable attention is being paid to reducing the impact of temperature, voltage, and process fluctuations [8], which can significantly affect the accuracy and dependability of the sensors. Ultra-low-power temperature sensors are also becoming more and more popular, which makes them perfect for Internet of Things applications and battery-operated devices.

Alongside these developments, scientists are investigating novel calibration methods to increase accuracy and reduce error margins. Real-time data analysis and enhanced sensor capabilities are made possible by integration with sophisticated signal processing techniques, which are also becoming more popular. Additionally, the use of more compact, smaller designs satisfies the need for electronic devices that are smaller in size while improving interoperability with modern integrated circuits. These innovations collectively pave the way for the next generation of temperature sensors, catering to a wide range of applications in healthcare, environmental monitoring, and industrial automation. [9,10]

II. SUB-THRESHOLD REGION OF MOSFET

In contrast to the linear and saturation areas, the current flowing through an NMOS transistor at the subthreshold region is controlled by a different equation, stating that this current can be written as follows: [8,9]

$$I_D = W/_L\, I_0 e^{\frac{V_{GS}-V_{th}}{mV_T}}\left[1 - e^{\frac{-V_{DS}}{V_T}}\right] \cong W/_L\, I_0 e^{\frac{V_{GS}-V_{th}}{mV_T}} \quad (1)$$

Where, $V_T = K_B T/_q$

W and L are representations of the width and length of the transistor in these equations, while the gate-to-source and drain-to-source voltages supplied to the transistor are indicated by VDS and VGS, respectively. The dependent parameter that is likewise affected by temperature is $I0$. Vth is the NMOS transistor's threshold voltage, m is the technology-determined subthreshold slope factor that depends on fundamental constants, where kB is the Boltzmann constant, q represents the elementary charge, and T denotes the absolute temperature [10,11].

Now, V_{th} can be written as,

$$V_{th} = V_{th0} - 2V_T ln\left(\frac{N_A}{ni}\right) \quad (2)$$

Where, V_{th0} is the threshold voltage is, NA is a carrier concentration, and ni is an intrinsic carrier concentration

Drain-induced barrier lowering (DIBL) is a crucial factor to consider while examining the threshold voltage Vth.[12] At larger drain voltages, this effect lowers the threshold voltage. The MOSFET's drain-to-source resistance and transconductance in the subthreshold region can be written as follows: [13,14]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{mV_T} \quad (3)$$

$$r_d = \left(\frac{\partial I_D}{\partial V_{DS}}\right) = \frac{mV_T}{\lambda_D I_D} \quad (4)$$

Where, λ_D is the DIBL coefficient

III. PROPOSED TEMPERATURE SENSOR

The proposed temperature sensor comprises five transistors arranged in a differential configuration, as depicted in Fig. 1. Transistors M3, M4, and M5 are configured to function as active resistors. Utilizing a small-signal model, it can be observed that MOSFETs operating as active resistors behave like simple resistors with an equivalent resistance of 1/gm [12]. In this configuration, transistors M3, M4, and M5 act as simple resistors. However, since they are operating in the sub-threshold region, the expression for their transconductance (gm) is described by Equation 3. Consequently, the resistance exhibited by M3, M4, and M5 can be expressed as follows.

$$r_0 = \frac{1}{g_m} = \frac{mV_T}{I_D} = \frac{m}{I_D} \times \frac{K_B T}{q} \quad (5)$$

From Equation 5, the resistance of the transistors shows a direct relationship with the absolute temperature.

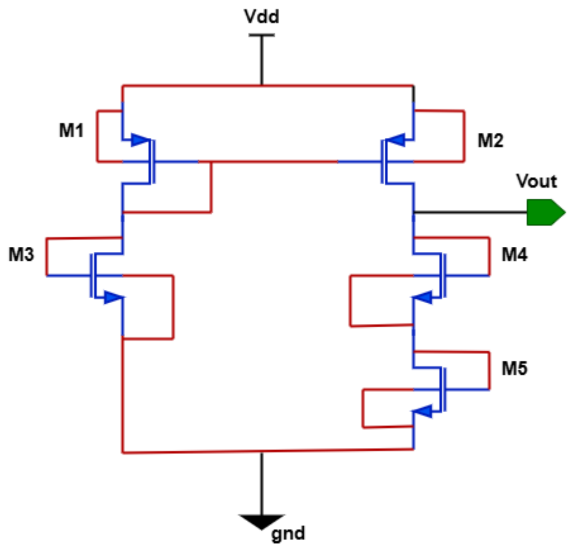

Fig. 1. Proposed Temperature Sensor Circuit

A current mirror replicates the current flowing through transistors M1 and M2 into M3, with amplification determined by the W/L ratios of M1 and M3. Likewise, transistors M4 and M5 draw distinct currents, and the output voltage Vout reflects the difference between the currents from these two sections. A pair of transistors is implemented on one side of the differential configuration design to increase the output voltage's linearity, which improves the circuit's accuracy and stability.

Electricity intake is of crucial to attention within the design of temperature sensors, in particular in low-power applications. When transistors operate inside the sub-threshold region, their current will increase exponentially with temperature. This behavior also extends to the biasing transistors, making them key participants in the circuit's usual strength dissipation. The cutting-edge inside the circuit is regulated by the biasing transistors, specifically by using their dimensions, as the dimensions of the biasing transistor without delay affect its current handling with potential and energy performance.

To gain ultimate overall performance, careful sizing of the biasing transistors is critical because it balances the alternate-off among electricity intake and the required sensitivity or dynamic range of the temperature sensor. Additionally, the usage of advanced layout strategies, along with using cascade current mirrors or dynamic biasing schemes, can further minimize energy dissipation while retaining high accuracy and linearity across a wide temperature range. Those considerations are especially essential for integration in present-day programs such as wearable devices, IoT structures, and different power-limited environments. Furthermore, sensors with smaller form factors are being developed because of improvements in fabrication techniques, which will enable their seamless integration into small and portable devices. Designers are also investigating the usage of cutting-edge materials and creative circuit topologies.

IV. SIMULATION RESULTS

The gpdk90 nm library and a +0.1V supply voltage are used to simulate the suggested temperature sensor inside the Cadence Virtuoso analog and digital design environment. The circuit, as illustrated in Fig. 1, exhibits a linear voltage response within the temperature range of -20°C to +100°C. At -20°C, the output voltage of the sensor is 14.0778 mV; even at a hundred°C, it increases to 29.9959 mV. The sensor achieves a sensitivity of 0.132 mV/°C, indicating a particular voltage variation with temperature. The output voltage of the sensor throughout one-of-a-kind temperatures is provided in Fig. 2. As is traditional, a mild discrepancy exists between the simulated effects and the best curve, known as errors. Fig. 3 shows the error of only ±0.1°C.

Because the circuit's temperature rises, its strength intake will also increase. At 100°C, the strength intake reaches 406.08 pW, while at room temperature (27°C), its miles notably lower at 80 pW. The connection between the circuit's power dissipation and temperature is depicted in Fig. 3, highlighting the sensor's energy-green overall performance throughout the range.

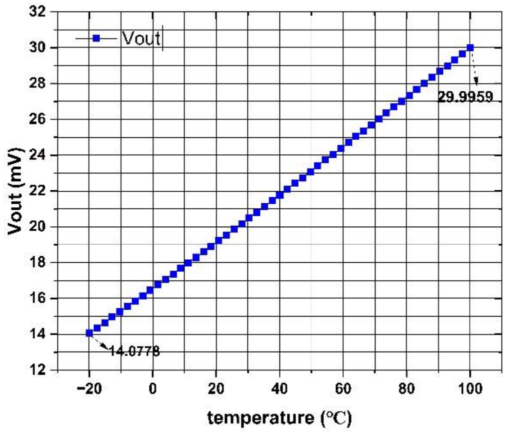

Fig. 2. Temperature Vs Voltage Graph

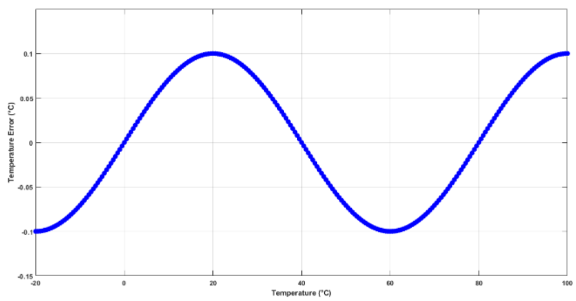

Fig. 3. Temperature Error (°C)

In real-world scenarios, power supply voltages are not perfectly constant and often exhibit slight offsets. To account for this, the circuit was simulated with a ±10 mV variation across a voltage range from ±0V to ±0.5V. The simulation results, shown in Fig. 4, indicate that the temperature curve shifts by +10 mV for every +10 mV increase in the power supply voltage.

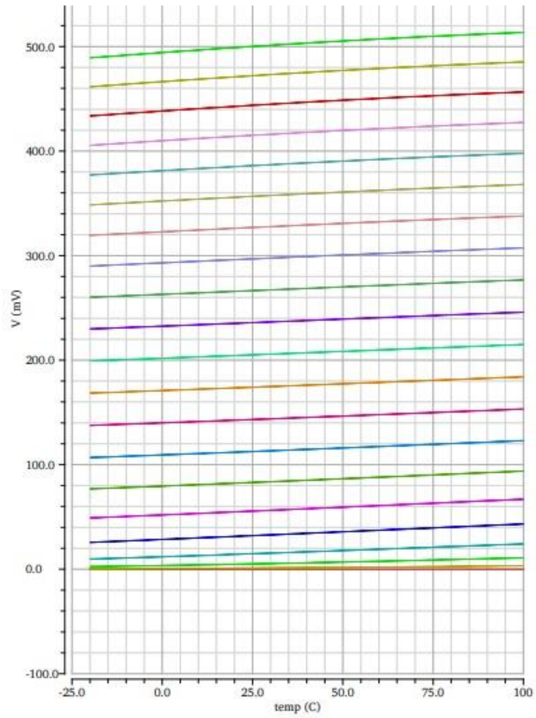

Fig.4. Temperature at various Voltage supplies between 0V and 0.6V with +10mV variation

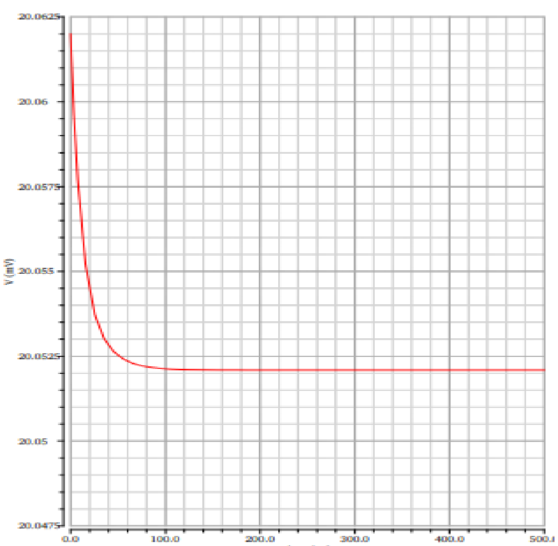

Fig. 5. Transient response of the proposed circuit

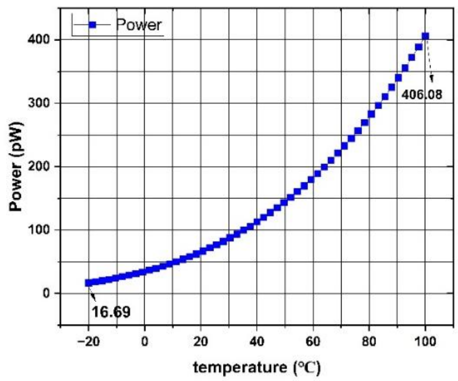

Fig. 6. Power Dissipation of Temperature Sensor

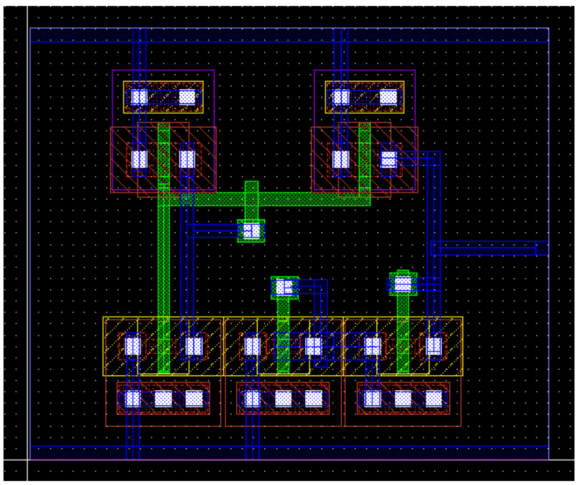

Fig. 7. Layout of Temperature Sensor of Fig1.

TABLE I. Performance analysis with existing Temperature Sensors

Parameter	[1]	[7]	[8]	Proposed Circuit
Technology (nm)	180	90	90	90
Power Supply (V)	1.4	1	1	0.1
Temperature Range (°C)	-40 to +125	-50 to +125	-55 to +155	-20 to +100
Power Consumption (W)	15u	25u	45n	406.08 p

The contributed work on the temperature sensor has been benchmarked in contrast to several previously designed circuits, as provided in Table 1. The contrast highlights that the proposed sensor famous drastically low energy dissipation, making it best for energy-restricted packages, which include IoT devices and transportable systems. The voltage output not simplest demonstrates excessive accuracy but also maintains outstanding linearity across the whole sensing range, ensuring dependable overall performance for precise temperature tracking.

Furthermore, among the designs compared, the proposed sensor's strength performance is unequaled, placing it apart as a distinctly optimized solution for low-electricity programs. The temperature range of the sensor spans over one hundred 50°C, covering a wide variety from -20°C to +100°C. This versatility makes it appropriate for each business and commercial environment.

The sensor's compact design, leveraging advanced CMOS technology, allows for seamless integration into current structures. Its robustness towards procedure, voltage, and temperature (PVT) versions further enhances its reliability and ensures consistent overall performance in diverse running conditions. These capabilities, blended with its minimal power requirements and wide sensing variety, make the proposed sensor a compelling choice for packages such as wearable devices, semiconductor testing, and environmental tracking structures.

V. CONCLUSION

The temperature sensor discussed in this newsletter operates with extremely low power consumption, measured in the picowatt range, whilst providing enormously accurate voltage outputs corresponding to the implemented temperature within its sensing range. With a sensing variety spanning from -20°C to +100°C, the sensor is ideal for diffusion of applications, together with commercial structures, wearable gadgets, and semiconductor technologies.

REFERENCES

[1] B. Gadogbe and R. Geiger, "A 15µW Low-Cost CMOS Smart Temperature Sensor," 2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS), Tempe, AZ, USA, pp.599-603,2023, doi:10.1109/MWSCAS57524.2023.10406048

[2] S. Chakraborty, A. Pandey, S. K. Saw, and V. Nath, "A 1.37nW CMOS temperature sensor with a sensing range of −25°C to 65°C," 2015 Global Conference on Communication Technologies (GCCT), Thuckalay, India, pp.

246-249,2015, doi: 10.1109/GCCT.2015.7342660.

[3] A. Rahali, M. Ouremchi, A. Elboutahiri, K. Elkhadiri, A. Tahiri, and H. Qjidaa, "Design of a Temperature Sensor With 0°C to 120°C Sensing Range for Li-Ion Battery Charger in 180 nm CMOS Technology," 2019 7th Mediterranean Congress of Telecommunications (CMT), Fez, Morocco, pp. 1-4,2019 doi: 10.1109/CMT.2019.8931349

[4] S. Joshi and P. K. Jain, "Design of 180nm CMOS linear temperature sensor," 2017 International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE), Bhopal, India, pp.469-472, 2017, doi:10.1109/RISE.2017.8378201.

[5] S. Pandey, J. S. Yadav, J. T. Mazumder and R. K. Jha, "CMOS Based Temperature Sensing Via Change in Threshold Voltage," 2023 3rd International Conference on Emerging Frontiers in Electrical and Electronic Technologies (ICEFEET), Patna, India, pp. 1-4,2023, doi:10.1109/ICEFEET59656.2023.10452249.

[6] Z. Tang, Z. Huang, X.-P. Yu, Z. Shi and N. N. Tan, "A 0.26-pJ·K2 2400-μm2 Digital Temperature Sensor in 55-nm CMOS," in IEEE Solid-State Circuits Letters, vol. 4, pp. 96-99, 2021, doi: 10.1109/LSSC.2021.3072989.

[7] M. Sasaki, M. Ikeda and K. Asada, "A Temperature Sensor with an Inaccuracy of −1/+0.8 ∘ C Using 90-nm 1-V CMOS for Online Thermal Monitoring of VLSI Circuits," in IEEE Transactions on Semiconductor Manufacturing, vol. 21, no. 2, pp. 201-208, May 2008, doi: 10.1109/TSM.2008.2000424

[8] D. Prasad, V. Nath, "An ultra-low power high-performance CMOS temperature sensor with an inaccuracy of -0.3 °C / +0.1ºC for aerospace applications, Microsystem Technologies", vol.24, issue-3, pp1553-1563, Springer Berlin Heidelberg, Online ISSN:1432-1858

[9] A. Pandey, V. Nath, ‘‘A CMOS Temperature Sensor and Auto-zeroing circuit with Inaccuracy of -1/+0.7 ºC between -30 ºC to 150 ºC Microsystem Technologies", vol. 23, issue-3, pp.4211-4219, Online May 2016, Springer Berlin Heidelberg, Online ISSN: 1432-1858, DOI: 10.1007/s00542-016-2968-2

[10] A. Pandey, V. Nath, "Study and Design of 40 nW CMOS Temperature Sensor for Space Applications", Vol-13 No.-3 pp 813-819, Sept. 2015, ISSN:1693-6930.

[11] S. Chakraborty, A. Pandey, and V. Nath, "A CMOS Temperature Sensor with -60 °C to 150 °C Sensing Range and ±1.3ºC Inaccuracy",2015.

[12] A. Pandey, J. Singh, R. Kundu, D. Ghosh, V. Nath, "A119nW CMOS Temperature Sensor for Space Applications", *International Conference CCSN-2013* organized by Dept. of ECE, PIET, Raurkela, Odissa, India from 22-24th Nov,2013.

[13] P. Chen, C. Chen, C. Tsai, and W. Lu, "A Time-to-Digital Converter Based CMOS Smart Temperature Sensor." IEEE J. Solid-State Circuits, vol. 40, no.8, pp. 1642-1648, August 2005.

[14] K. Woo, S. Meninger, T. Xanthopoulos, E. Crain, D. Ha, and D. Ham, "Time-domain CMOS temperature sensors with dual delay-locked loops for microprocessor thermal monitoring," IEEE Trans. Very Large-Scale Integration. (VLSI) Syst., vol. 20, no. 9, pp. 1590–1601, September 2012.

AUTHORS:

Rahul Kumar Raj received his BTech degree from Chandigarh Engineering College, Punjab, India, in 2020. He is pursuing MTech at the Department of Electronics and Communication Engineering, Birla Institute of Technology Mesra, Ranchi, Jharkhand, India. His areas of interest are low-power VLSI design and digital VLSI design.

Corresponding author E-mail: rahul702raj@gmail.com

Nikhat Anjum received her bachelor's degree in Electronics and Communication Engineering from the Institution of Engineers India (IEI), Kolkata, India, and her master's in technology in Electronics and Communication Engineering from Synergy Institute of Engineering and Technology, Dhenkanal, Odisha. She is currently working towards a PhD degree in Electronics and Communication Engineering at Birla Institute of Technology, Mesra, Ranchi. Her research interests are microelectronics, low-power very large-scale integration design, application-specific integrated circuit design, embedded system design, artificial intelligence & machine learning.

Email: nikhat.anjum2024@gmail.com

Vijay Nath received his BSc degree in physics from DDU University Gorakhpur, India in 1998, and PG Diploma in computer networking from MMM University of Technology Gorakhpur, India in 1999 and his MSc degree in electronics from DDU University Gorakhpur, India in 2001, and PhD degree in electronics from Dr. Ram Manohar Lohiya Avadh University Ayodhya (UP) and in association with CEERI Pilani (Raj), India in 2008. His areas of interest are ultra-low-power temperature sensors for missile applications, microelectronics engineering, mixed-signal design, application-specific integrated circuit design, embedded system design, cardiac pacemakers, internet of things, artificial intelligence & machine learning, and computational intelligence.
E-mail: vijaynath@bitmesra.ac.in