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Analog / Full Custom IC Design of Wilson Current Mirror

Rajapriyadharshini B, Renisha V, Shivani S, Bharath Kumar S and Latha P

Department of Electronics and Communication Engineering, St. Joseph's College of Engineering, Chennai, Tamil Nadu, India

ABSTRACT
This paper presents the design and implementation of an analog integrated circuit (IC) based on the Wilson current mirror topology. The design process was carried out using the Cadence Virtuoso tool suite. The initial phase involved creating the schematic in the Schematic Editor and generating a corresponding symbol to represent the circuit. A test bench was subsequently constructed using this symbol to enable simulation and performance evaluation. Input and output waveforms were obtained and analyzed to validate the functionality of the design. Additionally, the layout was generated and modified to meet design specifications. Physical verification, including Design Rule Check (DRC), Layout Versus Schematic (LVS), and RC extraction, was conducted using the Assura tool to ensure compliance with design rules. Finally, the design was prepared for fabrication through the generation of a Graphic Design System (GDS) file.

KEYWORDS
Integrated Circuit (IC); Design Rule Check (DRC); Layout Versus Schematic (LVS); Resistance-Capacitance (RC); Graphic Design System (GDS); Metal Oxide Semiconductor (MOS); Assura Verification (AV)

1. INTRODUCTION

The Wilson current mirror, introduced by George Wilson in 1967, is a pivotal topology in analog integrated circuit (IC) design, offering superior precision and performance over conventional current mirrors. Unlike the basic two-transistor configuration, the Wilson current mirror employs a three-transistor arrangement, significantly enhancing key performance metrics such as accuracy, output impedance, and immunity to base current errors.

Advantages of the Wilson current mirror include:

1. **Enhanced accuracy** due to its three-transistor configuration, which minimizes errors caused by base currents.
2. **High output impedance**, making it more stable and less sensitive to variations in load conditions.
3. **Reduced voltage headroom requirement**, allowing efficient operation in low-voltage designs.
4. An integrated **feedback mechanism** that dynamically adjusts for internal mismatches, improving overall precision and linearity.

Applications of the Wilson current mirror include:

1. **Biasing circuits**, where precise current control is essential.
2. **Operational amplifiers**, particularly in differential amplifier stages and precision current sources.
3. **Analog signal processing circuits**, such as mixers and modulators, which require accurate current

Despite its increased complexity and sensitivity to process variations, the Wilson current mirror remains an invaluable tool in precision analog IC design due to its superior performance characteristics.

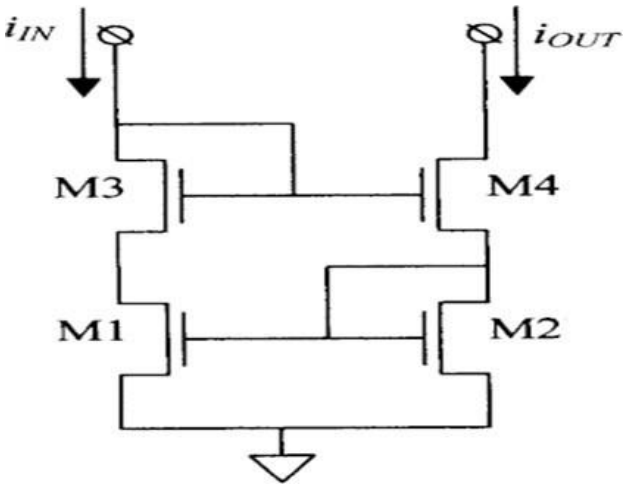

Fig. 1 Wilson Current Mirror

The Wilson current mirror is a sophisticated circuit configuration that employs MOSFET transistors to accurately replicate a reference current (I_IN) into an output current (I_OUT). It excels in maintaining high accuracy and stability even when the output voltage fluctuates.

The circuit comprises four MOSFET transistors, M1, M2, M3, and M4(From Fig.1). The reference current, I_IN, is injected into the gate of M1, establishing a current flow through M2 (I_OUT). To enhance accuracy, M3 and M4 are incorporated. M3 stabilizes the gate voltage of M1, minimizing the influence of output voltage variations. Consequently, M4 mirrors the

current through M3, further refining the accuracy of the output current.

This configuration offers several advantages. Firstly, it significantly improves accuracy by mitigating the impact of output voltage changes. Secondly, it exhibits a higher output impedance compared to basic current mirrors, making it less susceptible to load variations. Lastly, it can operate over a wider output voltage range while preserving accurate mirroring.

Properties of the Wilson current mirror include:

a) High Output Impedance
b) Improved Current Matching
c) Enhanced Linearity
d) Potential for Instability
e) Increased Complexity

This paper is organized as follows: Section 2 contains how the Wilson current mirror is implemented using MOS transistors in Cadence Virtuoso tool. The creation of the mirror symbol and generation of the waveforms are summarized in section 3. In section 4, the layout and verification process are shown. Then, the GDS file generation is given in Section 5. Finally, the conclusion is given in Section 6.

Here are the relevant equations based on the explanation [5-6]:

- Ideal MOSFETs: All transistors are assumed ideal.
- Saturation Operation: All transistors are in the saturation region.
  - $VoltageEquality: (V_{GS1} = V_{GS2}) and (V_{GS3} = V_{GS4})$.

Circuit Analysis:

Current Mirror Relations (M1 and M2):

The drain currents (I_{D1}) and (I_{D2}) for transistors (M_1) and (M_2), respectively, are given by:

$$I_{D1} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2 \quad (1)$$

$$I_{D2} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{tn})^2 \quad (2)$$

we can simplify the ratio of these currents as:

$$\frac{I_{D1}}{I_{D2}} = \frac{(W/L)_1}{(W/L)_2} \quad (3)$$

Current Mirror Relations (M3 and M4):

Similarly, for transistors (M_3) and (M_4), we have:

$$I_{D3} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_3 (V_{GS3} - V_{tn})^2 \quad (4)$$

$$I_{D4} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_4 (V_{GS4} - V_{tn})^2 \quad (5)$$

With ($V_{GS3} = V_{GS4}$), The Current Ratio is

$$\frac{I_{D3}}{I_{D4}} = \frac{(W/L)_3}{(W/L)_4} \quad (6)$$

Current Gain and Relationships:

$Assuming (M_1 = M_3) (i.e., ((W/L)_1 = (W/L)_3)) and (M_2 = M_4) (i.e., ((W/L)_2 = (W/L)_4)), the following relationships hold:$

- $InputCurrent: (i_{in} = I_{D1} = I_{D3})$
- $OutputCurrent: (i_{out} = I_{D2} = I_{D4})$

Thus, the current gain of the Wilson current mirror is[1]:

$$\text{Current Gain} = \frac{i_{out}}{i_{in}} = \frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \quad (7)$$

Summary of Equations:

- $OutputCurrent: (i_{out} = I_{D2})$
- $InputCurrent: (i_{in} = I_{D1})$
- $CurrentGain: (\text{Current Gain} = \frac{(W/L)_2}{(W/L)_1})$

Key Points:

- The Wilson current mirror allows precise current mirroring.
  - Current Gain is determined by the transistor geometry ratio = $\left(\frac{(W/L)_2}{(W/L)_1}\right)$ (8)

2. MOS TRANSISTOR IMPLEMENTATION OF WILSON CURRENT MIRROR

This session centered on the comprehensive design and schematic creation of an Analog Integrated Circuit (IC) using the Cadence – Virtuoso, a standard tool in the industry for analog circuit design. The process began by launching the Virtuoso log window, where an initial setup involved creating a dedicated library to organize project files systematically. Following the library setup, a schematic file was created, named

to reflect the circuit design and ensure streamlined referencing.

Using the Virtuoso Schematic Editor, the analog circuit was

meticulously constructed, with each component placed in alignment with specified design parameters.

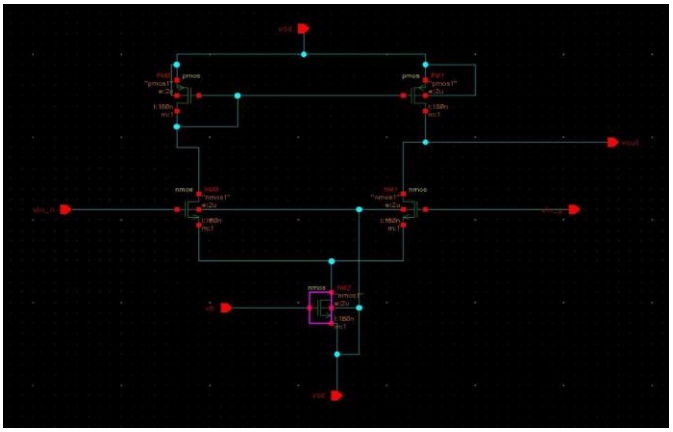

Fig. 2 Schematic Circuit of Wilson Current Mirror

From Fig.2 it can be inferred that this schematic utilizes five transistors, strategically combining two PMOS and three NMOS devices. While all transistors are initially placed, only two NMOS remain connected, forming the core of the mirror. We have three input pins, a supply voltage, a ground pin, and a dedicated output.[11]

This process included configuring component values and arranging connections to ensure signal integrity and adherence to circuit requirements. Careful attention was given to design rules and precise placement of components, supporting accurate integration of all schematic elements. This structured approach to schematic creation provided a robust foundation for further stages of IC design, ensuring that the circuit met all initial design objectives within the Cadence - Virtuoso environment.

3. SYMBOL AND WAVEFORM GENERATION

Following the completion of the circuit schematic, a symbol (Refer Fig.3) was generated for the circuit within the Virtuoso Schematic Editor. This custom symbol represented the designed circuit, enabling streamlined use in further simulations and test setups. For simulation, a test bench circuit was constructed in the Launch Editor window using the newly created symbol, which allowed for efficient setup of test parameters and configurations.

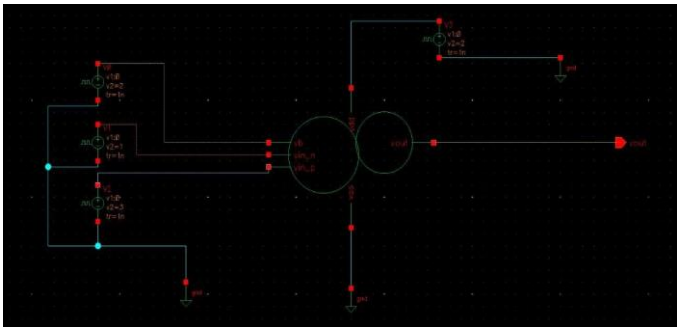

Fig. 3 Test Bench Circuit with created Wilson Current Mirror symbol

Input and supply voltages were defined as pulse sources, with specified voltage levels and time periods tailored to the simulation requirements. These pulse sources were configured to be either identical or varied, depending on the parameters of the desired test scenario. Additionally, DC voltage levels were set for each pulse, allowing for enhanced control and precision throughout the simulation process.

Upon completing the test bench configuration, the circuit was simulated to evaluate performance metrics. Input and output waveforms were observed, providing insights into the circuit's functionality and verifying that it met the desired operational requirements. This simulation process ensured the accuracy and integrity of the design, confirming that the circuit operated as intended within specified parameters.

Simulation and waveform analysis were conducted to reveal the circuit's behaviour under varied input conditions. Two primary responses were obtained:

1. **Transient Response:** The dynamic behavior of the circuit was visualized (refer fig. 4), displaying three input waveforms (each potentially set with different time periods) and the corresponding output waveform. In this instance, the first two inputs were configured with a 250 ns time period, resulting in similar waveforms, while the third input was set with a distinct 500 ns period.

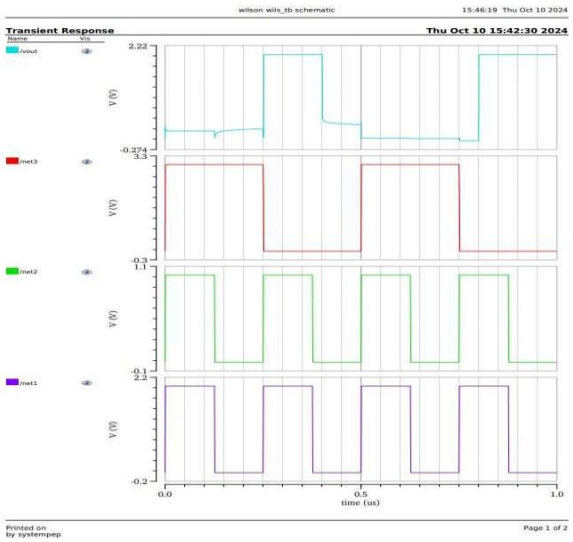

Fig. 4 Transient Response of Wilson Current Mirror

2. **DC Response:** This analysis examined the circuit's performance under constant voltage conditions. The output current's variation in response to changes in the second input voltage was observed, effectively demonstrating the mirroring effect in the circuit. (Refer Fig.5)

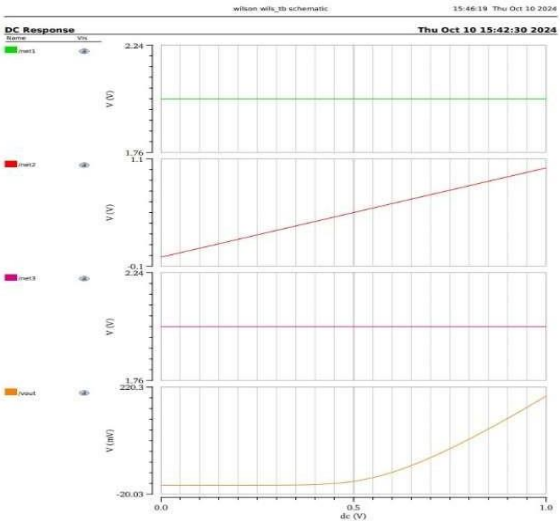

Fig. 5 DC Response of Wilson Current Mirror

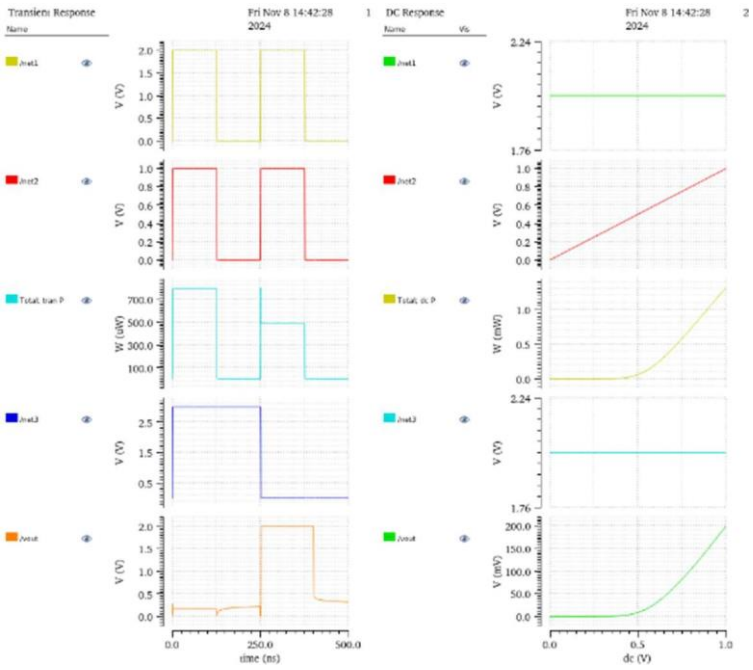

Fig. 6 Power Analysis Response of Wilson Current Mirror

4. LAYOUT CREATION AND VERIFICATION

The layout schematic (Refer Fig. 7) of a Wilson current mirror in Virtuoso Schematic Editor visually defines each component and connection in the circuit to ensure it meets the design specifications accurately. In creating the Wilson current mirror layout, precise attention to each component's placement, dimensions, and interconnections is crucial for achieving the desired current mirroring behaviour with high accuracy.

1. Transistor Layouts
   - Transistor Type: Typically, the Wilson current mirror uses MOSFETs, either PMOS or NMOS, depending on design requirements.
   - Placement and Matching: The transistors used for mirroring are placed closely and in parallel to ensure good matching. This reduces mismatch in threshold voltages and improves current mirroring accuracy.
   - Fingered Layouts: To improve performance and matching, each transistor can be laid out using a "fingering" technique. This involves breaking the transistor into smaller sections (fingers) that are placed symmetrically. Fingering also helps with thermal distribution, reducing variations caused by localized heating.

2. Metal Layers and Routing
   - Metal Layers: Virtuoso uses multiple metal layers to route connections, allowing for optimized signal flow and minimal interference. Each metal layer serves a specific purpose in the layout:
   - Lower Layers: Used for connecting source and drain terminals and for shorter, more localized connections.
   - Higher Layers: Used for power distribution and routing the input and output connections over longer distances to reduce resistance.
   - Contacts and Vias: Contacts and vias connect the transistor terminals (source, drain, and gate) to the metal layers. In Virtuoso, these are meticulously placed to minimize resistance and ensure robust connectivity.

3. Power Supply (Vcc) and Ground Connection
   - Vcc and GND Rails: The power and ground lines are typically placed in a grid structure or along the edges of the layout. They ensure that each transistor has direct and stable access to Vcc and GND, minimizing voltage drops across the circuit.
   - Width Optimization: Power lines are often made wider to reduce resistance, maintaining a stable supply voltage across the circuit.

4. Biasing and Reference Current
   - Reference Current Input: The layout includes a dedicated path for the reference current input. Proper isolation techniques are used here to prevent the reference path from picking up noise or interference from other parts of the circuit.
   - Gate Bias Connections: The gate terminals are typically connected to a shared node for the reference current. This shared connection is routed using low-resistance paths to ensure stable biasing and consistent current mirroring.

5. Output Node
   - Positioning: The output node is carefully routed directly from the mirror transistor. It is typically isolated from sensitive input nodes to prevent cross-talk and interference.

6. Symmetry and Matching Techniques
   - Layout Symmetry: Symmetry is maintained in the layout for matched transistors to ensure that they have identical electrical characteristics. Any asymmetry could cause mismatches, impacting the accuracy of current mirroring.
   - Common Centroid Layout: In sensitive designs, a common centroid layout technique is used. This method places transistors in a specific arrangement.

7. Spacing and Widths
   - The layout schematic adheres to foundry-specific design rules, which dictate the minimum spacing between components, trace widths, and alignment rules for specific fabrication technology. The layout schematic allows the Wilson current mirror to achieve stable current mirroring with high accuracy across various operating conditions.

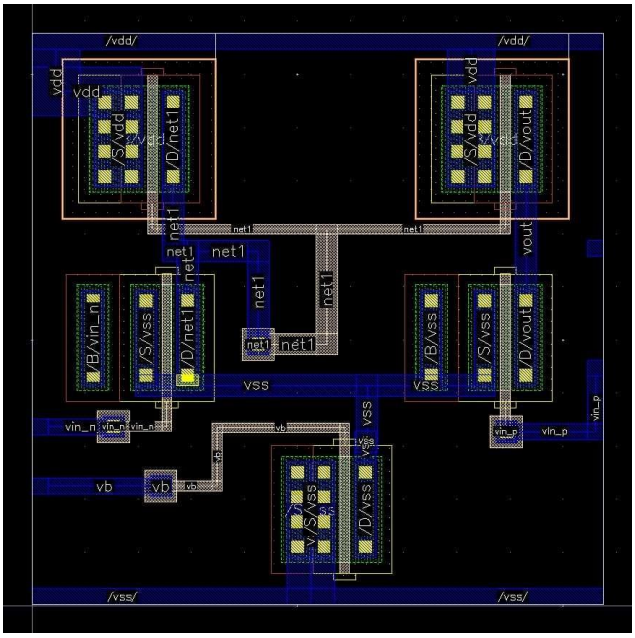

Fig. 7 Layout Schematic Circuit of Wilson Current Mirror

The physical verification process with Assura is a multi-step approach that ensures IC layouts meet critical standards for functionality, performance, and manufacturability. Each stage focuses on a different design aspect.

1. Design Rule Checking (DRC):
   - Purpose: Ensures layout adheres to foundry rules, which cover spacing, width, and layer overlaps.
   - Checks: Verifies minimum spacing between metal traces and diffusion regions, required widths to prevent reliability issues, and correct layer overlaps.
   - Outcome: Identifies shorts, open circuits, and misalignments, which are corrected iteratively until DRC compliance is achieved.

2. Layout vs. Schematic (LVS):
   - Purpose: Confirms that the layout accurately reflects the schematic, ensuring functional equivalence.
   - Checks: Matches components and connections between the layout and schematic, identifying discrepancies like missing components or incorrect wiring.
   - Outcome: Pinpoints and allows for correction of mismatches to ensure the layout maintains the intended design functionality.

3. Resistance-Capacitance (RC) Extraction and Analysis:
   - Purpose: Calculates parasitic resistances and capacitances that arise from materials and proximity in the layout.
   - Checks: Assesses resistances in metal paths and capacitance between nearby elements, critical for understanding real-world signal delays and interference.
   - Outcome: Helps designers simulate performance accurately, allowing for layout adjustments to mitigate issues like RC delays and signal crosstalk.

4. Assura Verified (AV) File Extraction:
   - Purpose: Generates an AV file containing detailed electrical properties, including parasitics, for post-layout simulation.
   - Contents: Documented parameters for each device, along with resistances and capacitances for accurate electrical behaviour representation.
   - Outcome: Enables realistic performance simulation, helping to predict real-world behaviour and assess design reliability.

After completing the layout, an extensive physical verification phase was performed using the Assura verification tool. This phase included three critical checks: Design Rule Check (DRC), Layout Versus Schematic (LVS), and Resistance-Capacitance (RC) extraction.

The DRC process was conducted to confirm that the layout complied with the stringent manufacturing guidelines, reducing the risk of fabrication errors.

The LVS check was then completed to verify that the layout accurately represented the original schematic, highlighting any discrepancies between the intended circuit design and its physical implementation.

The RC extraction was performed to analyze parasitic resistances and capacitances, providing a clear view of potential signal integrity and performance impacts.

Errors identified during these verification checks were meticulously addressed and corrected, ensuring that the layout met both the design specifications and fabrication requirements. Finally, a thorough review of the AV (Assura Verification) extracted file was conducted to verify the layout's integrity.

This inspection validated that the layout accurately matched the intended design parameters and confirmed its readiness for future steps in the IC design flow.

This comprehensive verification and correction process not only improved the quality of the design but also contributed to the robustness and reliability of the layout, paving the way for a successful fabrication and operation. Fig. 8 represents the AV extracted file after all these checks.

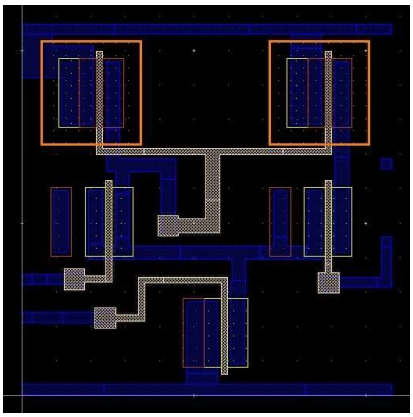

Fig. 8 AV Extracted Circuit of Wilson Current Mirror

These verifications ensured that the layout adhered strictly to fabrication design rules, accurately reflected the intended schematic, and accounted for all parasitic effects, guaranteeing fidelity in the final design. Each verification error was thoroughly addressed and resolved, ensuring compliance with both design intent and manufacturing specifications.

5. GRAPHIC DESIGN SYSTEM (GDS) FILE GENERATION

Upon completing the rigorous verification and refinement phases, the Graphic Design System (GDS) file was generated as the final deliverable in the layout design process.

This GDS file (Refer Fig.9), an industry-standard format for IC manufacturing, encapsulates all necessary geometric and layer-specific data, providing an exact blueprint for the integrated circuit's physical structure to be used by the semiconductor foundry.

The GDS file was prepared only after completing exhaustive verification stages, including Design Rule Check (DRC), Layout Versus Schematic (LVS), and Resistance-Capacitance (RC) extraction.

These verifications ensured that the layout adhered strictly to fabrication design rules, accurately reflected the intended schematic, and accounted for all parasitic effects, guaranteeing fidelity in the final design. Each verification error was thoroughly addressed and resolved, ensuring compliance with both design intent and manufacturing specifications.

The generation of this error-free GDS file marked the successful culmination of the design phase, rendering the project fully prepared for fabrication. By delivering a meticulously verified and optimized GDS file, we enabled a smooth transition to the foundry, minimizing the risk of post-manufacturing issues and ensuring the design's viability for production.

This step encapsulates the precision, rigor, and attention to detail required in IC design, setting the stage for the physical realization of the integrated circuit.

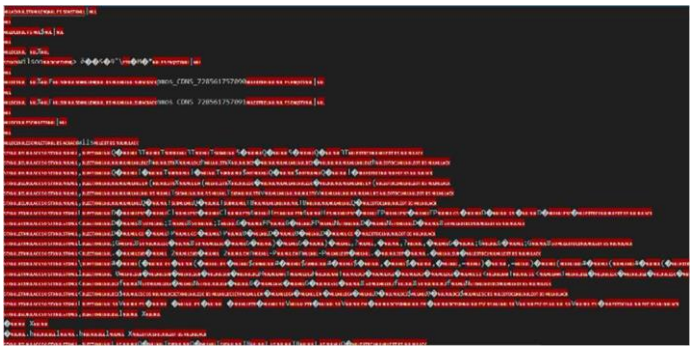

Fig. 9 Graphic Design System (GDS) file of Wilson Current Mirror

6. CONCLUSION

This study presents a comprehensive design and implementation of the Wilson current mirror circuit using the Cadence Virtuoso suite, underscoring its effectiveness in achieving precise current replication with enhanced accuracy and reduced error. The methodology spanned schematic creation, symbol generation, simulation, and layout design, followed by rigorous physical verification through Design Rule Check (DRC), Layout Versus Schematic (LVS), and RC checks using Assura.

Addressing limitations often encountered in conventional current mirrors—such as transistor mismatch, parasitic effects, noise, and temperature stability—our design utilized refined layout techniques and careful biasing.[3, 8, 10, 12, 13, 14, 15] The results indicate that the Wilson current mirror topology, optimized through these techniques, offers improved output impedance and stability under varied operating conditions, making it a strong candidate for applications demanding reliable current control and biasing accuracy. The successful generation of the final GDS file further demonstrates the circuit's readiness for fabrication and underscores the Wilson current mirror's continued relevance in modern analog IC design.

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AUTHORS:

Rajapriyadharshini B is currently pursuing her B.E degree from St. Joseph's College of Engineering, Chennai, Tamil Nadu, India. She has a 9.13 CGPA as of semester 4. Her areas of interest are analog VLSI design, digital VLSI design, physical design, design verification, React JS (Java Script) and Website Development.

Email: rajapriya091604@gmail.com

Renisha V is currently pursuing her B.E degree from St. Joseph's College of Engineering, Chennai, Tamil Nadu, India. She has an 8.38 CGPA as of semester 4. Her areas of interest are design verification in VLSI, digital VLSI design, analog VLSI design and Internet of Things.

Email: renisha4012@gmail.com

Shivani S is currently pursuing her B.E degree from St. Joseph's College of Engineering, Chennai, Tamil Nadu, India. She has a 9.10 CGPA as of semester 4. Her areas of interest are VLSI verification,

Bharath Kumar S is currently pursuing his B.E degree from St. Joseph's College of Engineering, Chennai, Tamil Nadu, India. He has a 7.50 CGPA as of semester 4. His areas of interest are analog, digital VLSI design, Embedded Systems Website Development and Internet of Things. Email: sbharath2003@gmail.com

P Latha received her B.E. degree in Electronics & Communication Engineering from GCT, Coimbatore, India in 1997 and M.E. degree in Applied Electronics from Sathyabama University, Chennai, India in 2004. She received her Ph.D. degree in the title "Reconfigurable System on Chip for WSN" from CEG, Guindy, Anna University, Chennai, India in 2015. Currently, she is working as an Associate Professor in the Department of Electronics and Communication Engineering, St. Joseph's College of Engineering, Chennai, India. Her interests are in Analysis and Design of Digital Circuits, Digital VLSI Design, Reconfigurable System on Chip, Wireless Sensor Network, Image Processing, Internet of Things and Cloud Computing.

Email: lathap@stjosephs.ac.in