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Design of Low Power Ambipolar CNTFET-Based Digital Adders

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ABSTRACT
This device having an intrinsic channel and Schottky barrier contacts have been taken into consideration because of the ongoing downscaling of MOSFETs. These transistors are ambipolar, which means that depending on the biasing circumstances, they can operate as either n-type or p-type devices. Due to their unique property of controlled polarity, Carbon Nanotube Field Effect Transistors (CNTFETs) are widely regarded as a possible candidate for future nanoscale transistor devices. As a result, ambipolarity gates based on CNTFETs require far fewer transistors in their circuit architecture than universal gates based on CMOS. In this study, we suggest building ambipolar CNTFET-based RCAs with universal gates (NAND and NOR) that have lower gate and power requirements than traditional CMOS libraries. Functional simulation utilizing Stanford CNTFET models in H- H-spice tools demonstrates the circuit's viability.

KEYWORDS
CMOS Ambipolarity, MOSFETs, Carbon Nano-Tube, NAND, NOR, Full Adder, RCAs

1. INTRODUCTION

Due to a variety of limitations, the miniaturization of silicon bulk devices/MOS-based devices is becoming more and more challenging [1-3]. This includes increased leakage current, sensitivity, and the short-channel effect. As a result, there is a need to replace silicon and look for new effective materials; carbon nanotubes (CNTs) are a promising candidate because they have high carrier mobility and current carrying capability. Carbon nanotubes (CNTs) are large molecules with hybridized carbon atom arrangements. They are fullerene carbon allotropes that are used in a variety of industries [4-5].

As the transportation of electrons in carbon nanotube field effect transistors (CNTFETs) is 1D ballistic, they are a superior alternative to MOS-based technology due to their high carrier mobility and enhanced electrostatic control. It has additional qualities including a high heat conductivity and a high tensile strength given its one-dimensional structure. Transistors are the fundamental building blocks of the digital world, and logic gates are employed to create them. As universal gates, NAND and NOR gates are utilized to implement any Boolean function [6- 9].

In comparison to standard MOSFETs, ambipolar CNTFETsoffer several benefits. One of their main characteristicsis their variable polarity, which permits the construction of ambipolar gates that may operate as either n-type or p-type devices depending on the biasing conditions.

Comparing ambipolar CNTFETs to conventional CMOS-based circuitscan result in reduced circuit complexity and power consumption. The remarkable electrical characteristics of ambipolar CNTFETs also include high mobility, low leakage current, andhigh on/off current ratios. They are perfect for high-speed and low-power applications because of these characteristics [10].

2. LITERATURE SURVEY

In the realm of carbon-based electronic devices, Xueyuan Liu (2022) [11] ventured into uncharted territory to explore the fascinating capabilities of ambipolar CFETs in configuring XOR logic and unraveling new dimensions in the realm of carbon-based logic circuits. Meanwhile, Junsung Park (2020) [12] embarked on a scientific expedition to overcome the challenges of detecting and analyzing terahertz (THz) radiation, delving into the realm of carbon nanotubes (CNTs) to craft highly sensitive and rapid CNT-based detectors and spectrometers, promising breakthroughs in compact and high-performance THz imaging and communication systems.

On a parallel path, Houda Ghabri (2017) [13] undertook a meticulous journey to bridge the virtual and physical worlds of carbon nanotube field-effect transistors (CNTFETs), developing an accurate SPICE model to seamlessly integrate CNTFETs into electronic circuits. Simultaneously, Soheli (2014) [14] undertook a quest to unravel the mysteries of CNTFETs, creating a precise SPICE model that captured the effects of band-to-band tunneling, ambipolarity, and quantum capacitance, enabling designers to optimize CNTFET-based circuits with unprecedented precision. Arijit Ray chowdhury

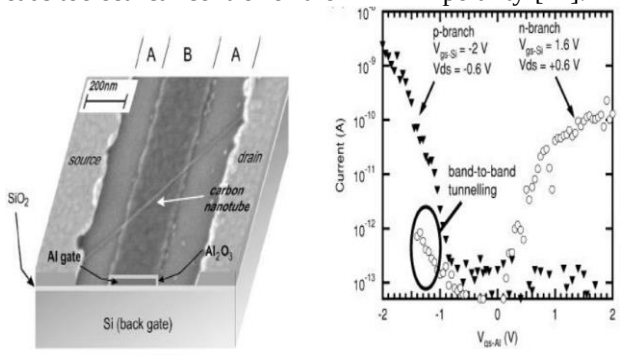
(2006) [15] embarked on an expedition to unlock the true potential of ambipolar CNTFETs, crafting dynamically reconfigurable logic cells that adapt to changing requirements by adjusting gate voltages. This flexibility revolutionized circuit design, unleashing the full potential of ambipolar CNTFETs. Moreover, researchers created a gate library that optimized circuit performance, minimized power consumption, and ensured reliable operation, advancing the design of ambipolar CNTFET-based integrated circuits [16-18].

Another group of researchers delved into the intricate worldof CNTFETs, accurately characterizing their complex electrical behavior, including ambipolarity and quantum capacitance. Their efforts yielded reliable models and techniques for integrating CNTFETs into reconfigurable logic circuits. Lastly, Arijit Raychowdhury (2006) [19] embarked on a captivating adventureto achieve the optimum transistor structure in CNTFETs for high-performance digital circuits, developing comprehensive models for precise simulation and optimization, unlocking the full potential of CNTFETs in digital circuit design.

I. AMBIPOLAR CONDUCTION IN CNTFETS

A. Ambipolar Structure and its Operation:

In Figure 1, when the transistor channel lengthis composed of intrinsic carbon nanotubes (CNTs), Schottky barriers form at the contacts and the devices exhibit ambipolar characteristics, which indicate conductivity for both electrons and holes as well as the manifestation of n-type and p-type behaviors. The gate field at the CNT-to-metal contact modulates the Schottky barrier's thickness, which leads toelectrical control of the device's polarity [12].

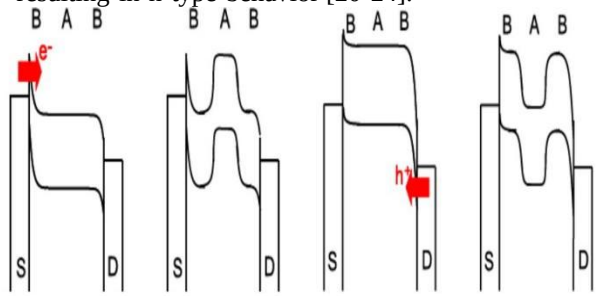


(a) View of ambipolar CNTFET (b) I_{ds}-V_{gs} curve of ambipolar CNTFET

Figure. 1. Observation and characterization of ambipolar CNTFETs include the following: a) SEM view of an ambipolar CNTFET, with area A serving asthe back gate and region B as the top gate. b) The $I_{ds}V_{gs}$ curve, with the top gate voltage fixed, shows the behavior of the device as either n-type or p-type depending on the polarity of the rear gate voltage [12].

Region A controls the current flow through the transistor, while Region B controls the polarity of the ambipolar carbon nanotube field-effect transistor. The ensuing behavior, which can be either n- or p-type, depends on the applied voltage.

In Figure 2, a band diagram is used to show the ambipolar CNTFET's operational concept [13]. The transistor's Schottky barrier exists at the drain and source contacts can be made thinnerby choosing the appropriate contact in region B. When a suitably positive voltage (V+) is applied at the electrode controlling area B, the Schottky barrier becomes transparent to tunneling electrons, resulting in n-type behavior [20-24].



(a) $V_{PG}>0, V_{CG}>0$ (b) $V_{PG}>0, V_{CG}<0$ (c) $V_{PG}<0, V_{CG}<0$ (d) $V_{PG}<0, V_{CG}>0$

Figure 2. An Ambipolar CNTFET's band diagram: (a) The CNTFET acts like an n-type device when VPG>0. There is an electron current when VCG>0. (b)The passage of electrons is blocked by the n-type device. (c) The CNTFET acts like a p-type device when VPG<0. A hole current as majority carrier when VCG <0. (d) The hole current flow is blocked by the p-type device [13].

On the other hand, p-type behavior results from the Schottky barrier being transparent to tunneling holes when thesame voltage (V-) is sufficiently negative and big. Becausethe barrier is too thick for both electrons and holes at this voltage, which would result in poor conduction across thetransistor, a voltage (V_{ds}) applied between the drain and source is minimized with a polarity gate bias $V0=V_{ds}/2$.

The conduction is likewise subpar if the polarity gate isleft disconnected. By creating a strong potential barrier in the channel's midsection due to the applied voltage in region A, any possible current flow may be restricted. Meanwhile, the polarity of the device is determined by the voltage applied in area B (Figure 2).

B. Ambipolar CNTFET Transistor

Due to the overlapping of electron and hole currents, which enables them to operate as either an n-type or p-type device, ambipolar CNTFETs operate by utilizing both electrons and holes as charge carriers. In the channel of the ambipolar CNTFET, a semiconducting carbon nanotube serves as a link between two metal electrodes. MOSFETs only use either electrons or holes as the majority carriers (n- or p-type), but ambipolar CNTFETs can operate with both electrons and holes. Ambipolar CNTFETs outperform MOSFETs in terms of flexibility and power consumption thanks to thischaracteristic [25-27].

This work describes a real-world application of an ambipolar CNTFET (Figure 3), which makes use of the back gate as the polarity gate and the transmission gate approach. The ambipolar transistor works as an NMOS

when the polaritygate is set to logic "0", and as a PMOS when it is set to logic "1". The ambipolar transistor's symbol and multiple modes of operation are shown in Figure 4.

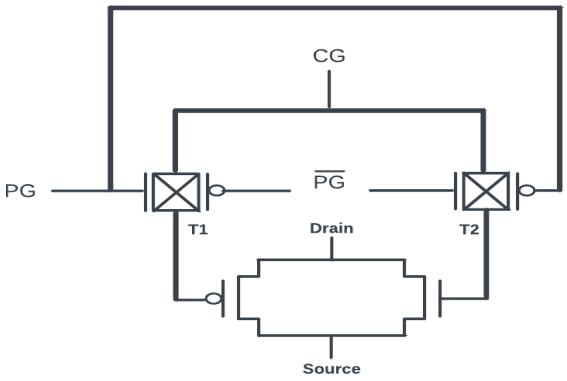


Figure 3. Functional model of an ambipolar CNTFET, CG denotes the Control Gateor Gate and PG denotes the Polarity Gate

From a logical design perspective, an ambipolar CNTFET can function as an n-type or p-type transistor depending onthe voltage applied to its polarity gate (PG) shown in Figure 4. Specifically, a positive voltage applied to PG causes it to operate as an n-type transistor, while a negative voltage applied to PG makes it a p-type transistor. Thus, when designing logic circuits with ambipolar CNTFETs, a "0" logic at PG is used for n-type operation, while a "1" logic at PG is used for p-type operation.

3. IMPLEMENTATION AND SIMULATION RESULTS

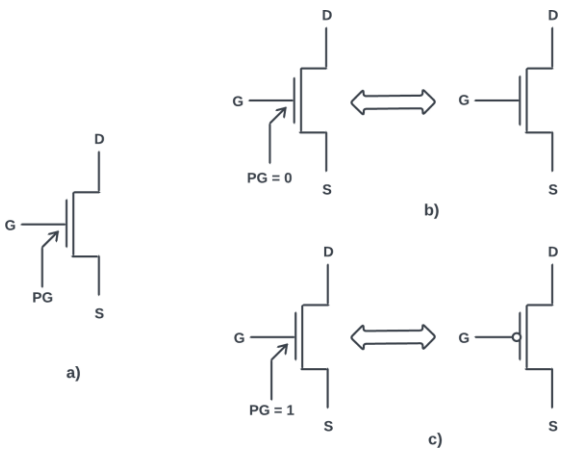


Figure 4. An illustration of an Ambipolar CNTFET's symbol and operating modes. In a), the device symbol is displayed, and in b), the n-type or p-type operation modes are shown.

A. Ambipolar CNTFET NAND and NOR gates

A schematic for both ambipolar CNTFET-based universal gates is illustrated below. An ambipolar CNTFET and a conventional p-type CNTFET are both employed in the ambipolarNAND gate, and both source terminals are coupled to the supply voltage V_{dd}. While the ambipolar NOR gate makesuse of an n-type CNTFET linked to the ground and an ambipolar CNTFET connected to Vdd. Further plotting of the simulationdata is done to confirm the devices' functionality.

The working of the ambipolar CNTFET NAND gate is briefly demonstrated in the section below.

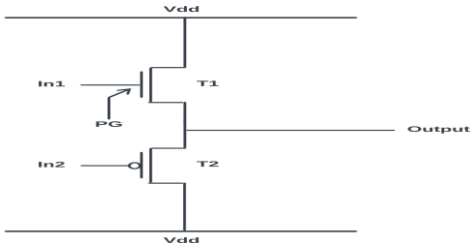


Figure 5 Circuit diagram of ambipolar CNTFET NAND gate

The ambipolar CNTFET is used in four different scenarios in the suggested circuit architecture. In the first scenario, the ambipolar transistor operates as a p-type CNTFET and is turned on when Inputs 1 and 2 are both low and PG is high.As a result, the lower p-type CNTFET transistor stays on, maintaining the circuit's potential. As a result, the output is V_{dd} or high.

In the second scenario, Input 1 and 2 are high and low respectively. The ambipolar transistor operates as an n-type CNTFET due to PG being set to low and is turned on. However, the bottom transistor remains active and continues to function as a p-type CNTFET. The result is a high output.

In the third scenario, Input 1 is low while Input 2 is high. The ambipolar transistor operates as a p-type CNTFET dueto PG being set too high and is turned off. However since the bottom transistor is turned off, it results in a high output.

In the fourth scenario, the ambipolar transistor performs likea p-type CNTFET and is turned off when Inputs 1 and 2 are both at logic high and the polarity gate is also at logic high. As a result, the lower transistor is also turned off, bringing the circuit's potential to zero and producing a grounded output, asa logic low.

TABLE I
TRUTH TABLE OF AMBIPOLAR CNTFET NAND GATE

Input 1	Input 2	PG	Output
0	0	1	1
1	0	0	1
0	1	1	1
1	1	1	0

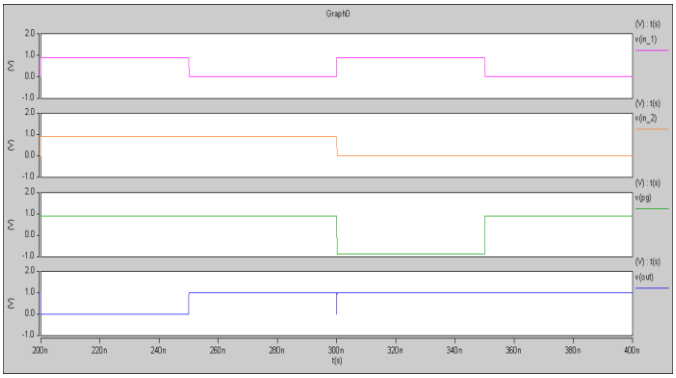


Figure 6. Simulated waveform of ambipolar CNTFET NAND gate

The working of the ambipolar CNTFET NOR gate is briefly demonstrated in the section below.

The ambipolar CNTFET is used in four different scenarios in the suggested circuit architecture. In the first scenario, Input1 as well as Input 2 are at logic high, the circuit's ambipolar transistor is set as p-type CNTFET as PG is high. The n-type CNTFET, the bottom transistor, is disabled and generates a Vdd or high output.

In the second scenario, the bottom transistor remains off when Input 1 is high and Input 2 is low, while the ambipolar transistor operates as a p-type CNTFET as PG is set to high and turns off. This results in a grounded or low output.

In the third scenario, Input 1 is set as low while Input 2 is set as high. The ambipolar transistor in the circuit behaves as n-type CNTFET and since PG is low, it turns off. An outputof low is produced as a result of the lower transistor, an n-type CNTFET, turning on in the background.

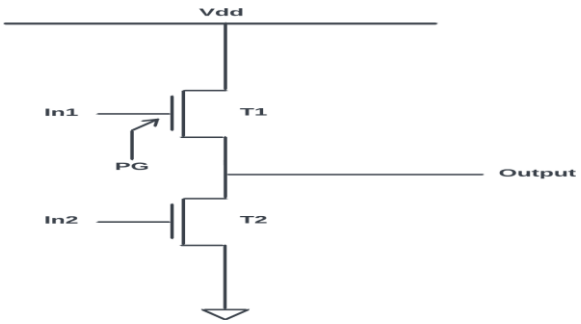


Figure 7 Circuit diagram of ambipolar CNTFET NOR gate

In the fourth scenario, the ambipolar transistor behaves as p-type CNTFET and switches off, while the lower transistor turns on when Inputs 1 and 2 are both high and PG is high. Low output is the result of this.

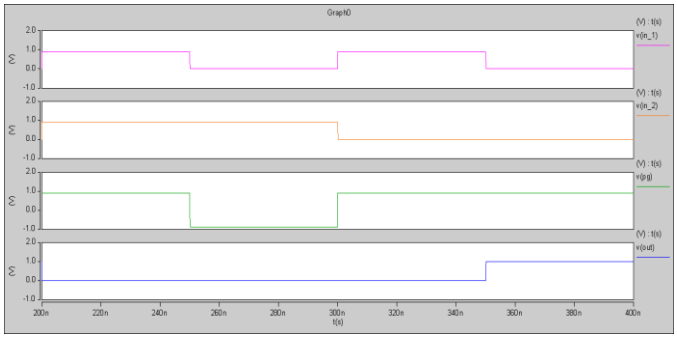


Figure 8 Simulated waveform of ambipolar CNTFET NOR gate

TABLE II
TRUTH TABLE OF AMBIPOLAR CNTFET NOR GATE

Input 1	Input 2	PG	Output
0	0	1	1
1	0	1	0
0	1	0	0
1	1	1	0

It is evident from the above comparison that CMOS-based universal gates require a significantly higher numberof transistors, which in turn takes up more space and higher power consumption, compared to ambipolar CNTFET-based universal gates.

B. Ambipolar CNTFET based Full adders and RCAs

A full adder circuit using ambipolar transistors is implemented in HSPICE which is shown in Figure 13.

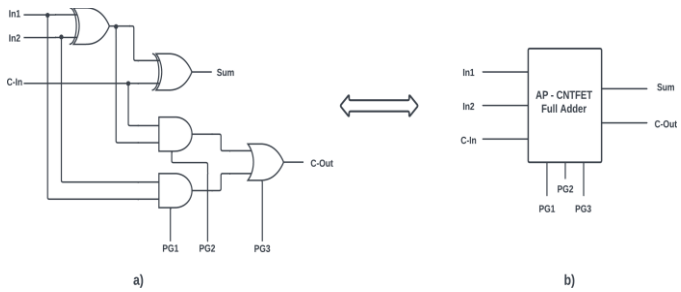


Figure 9 Ambipolar CNTFET full adder a) Circuit diagram b) Equivalent block diagram

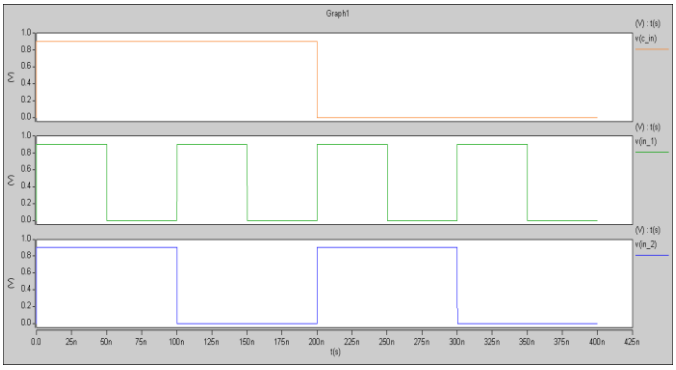


Figure 10 Simulated waveform of input in Ambipolar CNTFET Adder

Here, a novel design for a full adder is presented. This proposed full adder is fabricated utilizing two XOR gates based on CNTFETs, two ambipolar AND gates, and an ambipolar OR gate. The XOR gates were constructed using regular CNTFET architecture while the ambipolar NAND andNOR gates shown earlier were transformed into AND and OR gates by incorporating an inverter circuit. The proposed full adder has eight terminals, out of which three are newly introduced polarity gates. This architecture offers a significantreduction in the number of transistors required at the expense of additional input lines.

The subsequent design is an instantiation of ambipolar Ripple Carry Adder (RCA) utilizing the previously described full adder as depicted in Figure 13

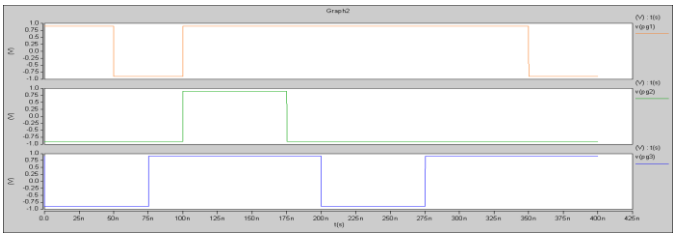


Figure 11 Simulated waveform of PG gates in ambipolar CNTFET full adders

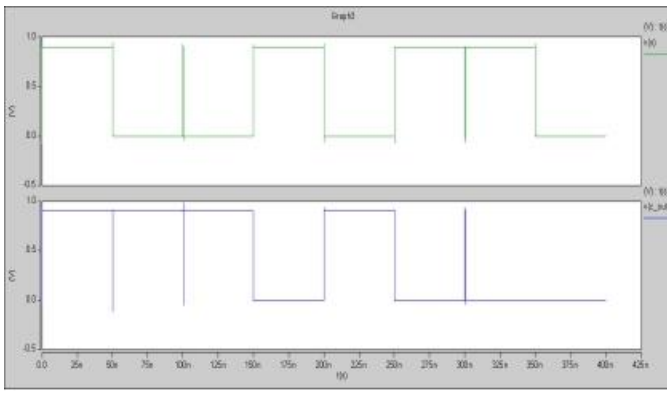


Figure 12 Simulated waveform of output in ambipolar CNTFET full adder

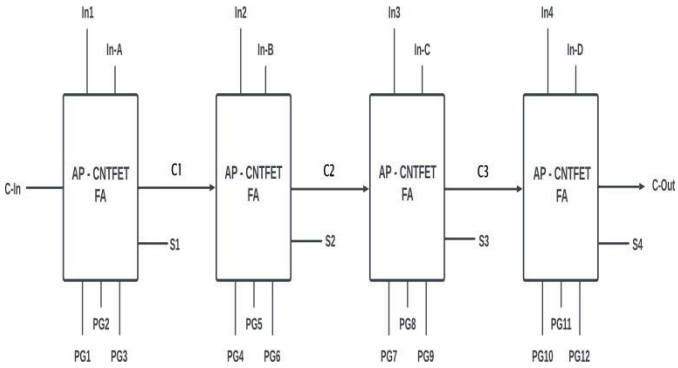


Figure 13 Block diagram of ambipolar RCA

The novel ambipolar 4-bit Ripple Carry Adder (RCA) isan extension of the ambipolar full adder. This RCA uses a combination of the proposed full adder and additional polarity gates to perform the addition of two 4-bit numbers. The proposed RCA consists of four full adders connected in a cascade. The RCA architecture also has an additional 12 polarity gates. The RCA operates by using the carry-out bit from each full adder to generate the carry-in bit for the next full adder.

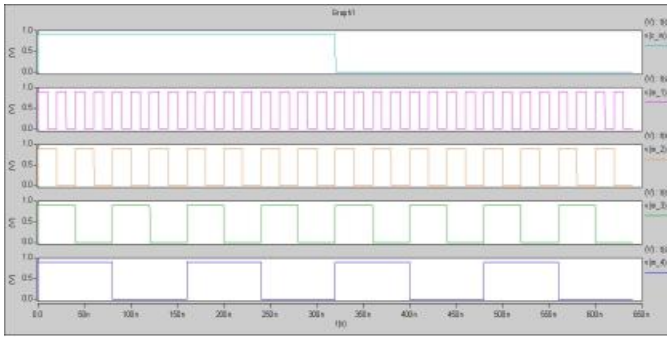


Fig. 14. Simulated waveform of 1st four inputs along with input carry inambipolar CNTFET RCA

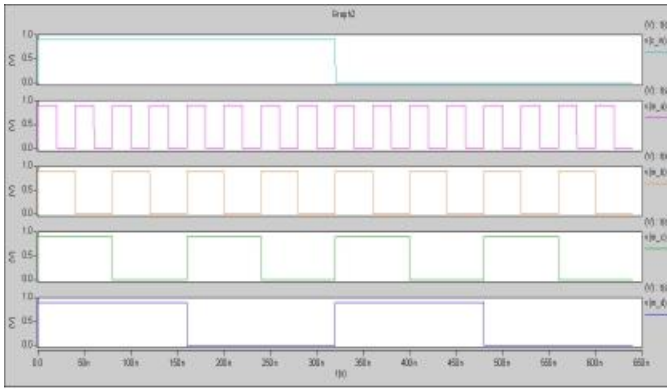


Fig. 15. Simulated waveform of 2nd four inputs along with input carry inambipolar CNTFET RCA

The advantages of the proposed ambipolar full adder andthe 4-bit RCA are its low power consumption, high-speedoperation, and reduced transistor count compared to

other reported designs. The use of ambipolar transistors also allows for a more efficient design with fewer transistors and reduced power consumption.

C. Operating Parameters:

In the first paragraph, the technical details of CMOS logic gates are presented. In the second paragraph, the technical details of ambipolar CNTFETs-based universal gates, full adder, and RCA are described. The MOSFET-based devices were designed with specific parameters: VDD = 0.9 V and a channel width of 45 nm.

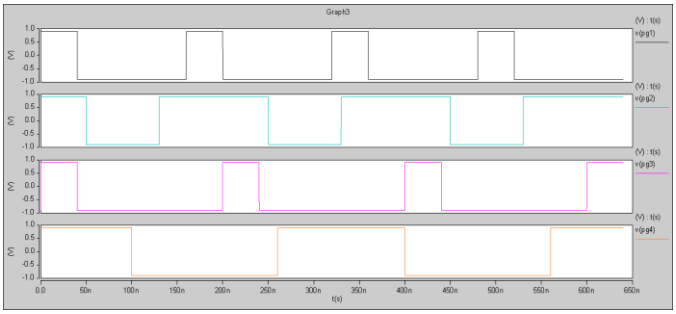


Figure 16 Simulated waveform of 1st four polarity gate inputs in ambipolarRCA

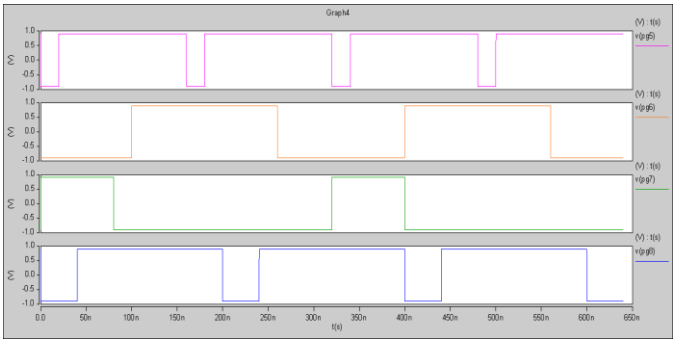


Figure 17 Simulated waveform of 2nd four polarity gate inputs in ambipolarRCA

The 45 nm technology node of the BSIM v4.8.1 Berkeley Predictive Technology model was used to simulate these MOSFETs.

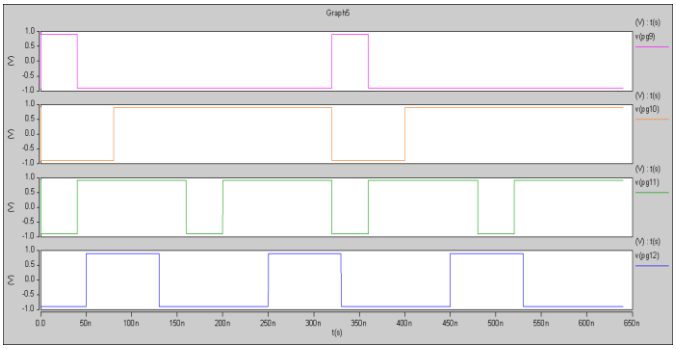


Figure 18 Simulated waveform of last four polarity gate inputs in ambipolarRCA

The Stanford CNTFET model was used to simulate the proposed ambipolar CNTFET devices. The simulation was conducted under the following parameters: VDD = 0.9 V, Channel Width = 45 nm, Effective Mean Free Path (L_{geff})= 200.0 nm, Pitch (S) = 20 nm, Tube Chirality = (19, 0),

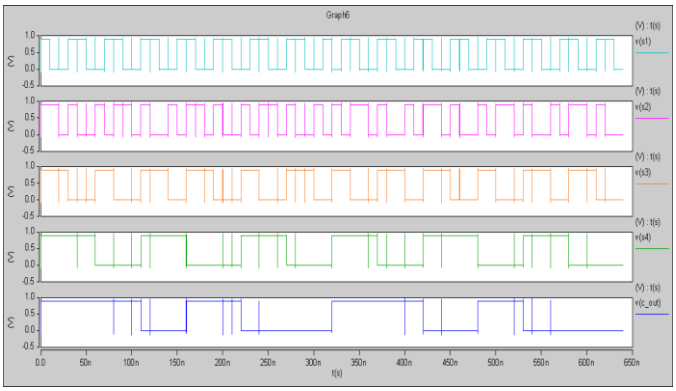


Fig. 19. Simulated waveform of output in ambipolar CNTFET RCA

No. of carbon nanotubes used (N) = 3, Diameter of carbon nanotube = 1.5 nm, Dielectric Constant (Kox) = 16, and Top Gate Dielectric Material Thickness (Hox) = 4 nm.

D. Discussions and Further enhancements

The proposed ambipolar CNTFET-based full adder and RCA have a reduced number of transistors as compared to MOS-based devices, which leads to a reduction in circuit complexity. The smaller size of CNTFETs allows for a higher density of transistors on a chip, which is further increasedby the reconfigurability of ambipolar CNTFETs leading to a smaller footprint of the circuit. This is especially important forapplications where miniaturization is critical, such as portable devices.

TABLE III
COMPARISON BETWEEN MOSFET AND AMBIPOLAR CNTFET NAND GATE

Parameters	MOSFET NAND Gate	Ambipolar CNT-FET NAND Gate
No. of Transistors required	4	2
Channel Length	45nm	45nm
Avg. Power Consumption	1.1548 µW	0.16446 µW

In the proposed architecture, the performance of logic gate circuits and data path logic circuits designed using ambipolar transistors is compared with that of CMOS architecture. It is found that the switching times and average power consumed by the gates designed using ambipolar transistors are lower than those designed using CMOS transistors. The comparison results are presented in a

tabulated format.

TABLE IV
COMPARISON BETWEEN MOSFET AND AMBIPOLAR CNTFET NOR GATE

Parameters	MOSFET NOR Gate	Ambipolar CNTFET NOR Gate
No. of Transistors required	4	2
Channel Length	45nm	45nm
Average Power Consumption	1.3482 µW	0.1948 µW

TABLE V
COMPARISON BETWEEN MOSFET AND AMBIPOLAR CNTFET FULL ADDER

Parameters	Asma [1]	MOSFET	Proposed Ambipolar CNTFET
No. of Transis-tors required	28	34	28
Channel Length	45nm	45nm	45nm
Avg. Power Consumption	0.844W	4.3065 µW	1.8066 µW

TABLE VI
COMPARISON BETWEEN MOSFET AND AMBIPOLAR CNTFET RCA

Parameters	MOSFET	Ambipolar CNTFET
No. of Transistors required	136	112
Channel Length	45nm	45nm
Avg. Power Consumption	0.1126 mW	0.1876 mW

The polarity gates, which are extra terminals apart from the input terminals, increase in number with the increase in the number of gates, leading to the requirement for more input lines. Moreover, precise synchronization is needed to switch the function of the ambipolar CNTFET to obtain the intended output using polarity gates. In the future, efforts will be focused on developing advanced switching and synchronizing circuits that can eliminate overlapping polarity gate signals, thereby reducing the number of inputs required.

4. CONCLUSION

The analysis and development of the H-spice model of CNTFETs are discussed briefly in this paper. It discusses the simulations of NAND and NOR gates and presents a comparison between different gate designs. The adoption of ambipolar NAND and NOR gates reduces power consumption by 7.041% and 6.914%, respectively.
The study also includes the circuit designs of a Full Adder and RCAs using both MOSFET and ambipolar CNTFET technologies. These designs were functionally verified, and their performance was compared. The results show a decrease of 2.384% in power consumption for thefull adder using ambipolar CNTFETs. In comparison, the RCA showsa slight increase of 1.66% due to the additional transistors required for implementing the ambipolar transistor.
The findings indicate that ambipolar CNTFET-based devices require fewer transistors compared to MOS-based transistors while delivering similar performance. This allows for a greater number of logic gates to be accommodated within the same chip area, enhancing overall system performance and speed. These circuits offer the potential to perform a wide range of functions within a limited chip area, thereby increasing overall system efficiency.

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