ISSN: 2584-0495 Vol. 2, Issue 4, pp. 745-752

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

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Cite as: Anvekar, S., Anusha, A. D., Giriraddi, G., Hegde, B., & Kotabagi, S. (2024). Single Stage Folded-Cascode Operational Amplifier. International Journal of Microsystems and IoT, 2(4), 745-752. https://doi.org/10.5281/zenodo.11654752

Published online: 22 April 2024

DOI: https://doi.org/10.5281/zenodo.11654752

International Journal of Microsystems and IoT
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Single Stage Folded-Cascode Operational Amplifier

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ABSTRACT
This paper mainly concentrates on designing a single-stage folded cascode op-amp with UMC 180nm technology. The amplifier operates seamlessly within the confines of a 1.8V power supply, shows a DC gain of 55dB, a phase margin of 66.87 degrees, and the amplifier's bandwidth is reported at 222kHz (-3dB) for a 1pF load. It works with ICMR range from 1.6V-0.8V. The proposed structure yields medium gain and wide output swing ranging from 300mV to 1.4V.

KEYWORDS
Current mirror; Folded Cascode; Operation-amplifier (Op-amp); Wide swing.

1. INTRODUCTION

The design of high-performance operational amplifiers (op amps) holds significant importance in the realm of analog integrated circuits, as it directly influences the functionality of circuits and systems. Over time, various op-amp topologies like telescopic, OTA, and so on have been developed using CMOS technology to attain high gain and optimize the performance parameters of an op-amp. One such topology is the folded cascode operational amplifier, which aims to enhance practical op-amp performance by improving parameters such as gain, phase margin, bandwidth, and output swing.

In modern applications, there is a growing demand for amplifiers exhibiting both high DC gain and bandwidth. For instance, in high-speed and high-resolution analog-to-digital converters (ADCs), operational amplifiers are required to possess high DC gain and high unity-gain frequency to meet the accuracy and rapid settling requirements of the system.

This paper presents an investigation into the folded cascode operational amplifier topology. Firstly, the concept of this topology will be elucidated, followed by a presentation of the circuit design proposed for this study. Subsequently, the results obtained from simulations will be analyzed and discussed in detail.

1.1 Motivation

The folded cascode op-amp topology is ideal for high performance applications requiring high gain, low output impedance, and high voltage swing. Its cascade stage minimizes the Miller effect, ensuring high gain. The folded cascode stage, with multiple parallel transistors, reduces effective output impedance and maintains signal integrity. This topology is suitable for applications that require high signal amplitude without distortion and improved bandwidth and stability in high-frequency applications. However, choosing the right op amp topology depends on specific requirements such as power consumption, cost, and system design considerations.

1.2 Objectives

Design a single stage folded cascode operational amplifier with specified performance criteria and focus on achieving a high output swing.

2. LITERATURE SURVEY

Gate-driven FCOTA operates in strong inversion, employing complementary PMOS and NMOS pairs for rail-to-rail ICMR. Cascode load structure enhances gain, enabling versatile trans fer functions. Simulated in UMC 0.18µm CMOS, it shows 93.6µW power and 6.03MHz GBW [1]. The article highlights a folded cascode BJT current source with high performance in output resistance, voltage swing, and frequency response. Using dual pnp-npn current mirrors, it achieves constant output current, 71Mohm output resistance, and 40kHz bandwidth [2]. Exploring folded cascode current source with dual pnp npn network for improved output impedance and bandwidth. Simulations confirm stability, prompting exploration in low power MOSFET integration for analog ICs [3]. The compact folded cascode operational amplifier prioritizes EMI immunity, showing a maximum 6.6 mV output offset voltage across 1 MHz to 1 GHz frequencies. This resilience, coupled with key specifications akin to robust designs, suits critical signal integrity applications. [4]. Introducing IRFC OTA with DFC compensation in 0.18µm CMOS, achieving 157MHz unity gain frequency, 90.1dB DC gain, and improved slewing. Ideal for high-speed applications [5].

A fully differential output is preferred due to its ability to increase the maximum achievable voltage swings and provide higher immunity to environmental noise compared to single ended configurations [6]. This paper aims to develop a high-temperature op-amp for Analog-to-Digital Converters (ADCs) using silicon carbide ICs. Operating from 25°C to 300°C, it meets performance requirements. Simulation results show optimal performance at 300°C, confirmed across different process and temperature conditions (300TF and 25TF). Specifications closely match expected values despite variations [7]. The paper introduces a high-speed operational amplifier design with complementary folded cascode, achieving a maximum slew rate over 20,000 V/µs while overcoming traditional output current limitations and maintaining stable transient parameters [8]. The paper presents a novel CMOS folded cascode op-amp tailored for LDO applications, demonstrating high PSRR and gain like a two-stage op-amp. Implemented in 0.18µm technology, it achieves a DC gain of 72.0404 dB, a phase margin of 62.4636 degrees, and a PSRR of 72.0966 dB under a 1.8 V supply [9].

The paper introduces a high-performance folded cascode amplifier featuring a figure of merit (FoM) of 5540 MHz·pF/mA, demonstrating effective functionality in driving capacitive loads for low-power applications [10]. The article presents an innovative Folded Cascode Op-Amp design incorporating positive feedback to enhance DC gain while preserving frequency response. It tackles issues related to voltage headroom, stability, and linearity, surpassing conventional designs in performance [11]. The article compares 2 architectures of folded cascode recycling and complementary and their parameters. It discusses how the feedback system helps to improve the circuit [12]. The article has the results of the Folded cascode OTA and describes how it is better than the telescopic opamp in the matter of output swing and better than other architectures in the matter of speed [13]. The article discusses the methodology to increase the gain of a recycle folded cascode OTA. It compares the parameters with the recycling folded cascode OTA and modified one [14]. The paper introduces a modified version of the folded cascode amplifier, called Recycling Folded Cascode (RFC), which improves performance while minimizing power usage, especially suitable for low-voltage scenarios. By employing multipath schemes and reusing idle transistor bias currents, the RFC achieves superior transconductance and slew rate with decreased power consumption, as validated through simulations in CMOS technology [15]. The journal suggests a method to bolster the resilience of fully differential folded cascode opamp by tackling issues related to hidden positive feedback and start-up problems. This proposed solution aims to reduce the likelihood of latch-up occurrences, resulting in enhancing reliability during large-scale production. By using a start-up circuit grounded on current comparison principles, the solution adeptly overcomes start-up hurdles without substantially augmenting power consumption. These improvements fortify the stability and dependability of fully differential folded cascode opamp in CMOS technology, ensuring consistent performance across applications [16]. The methodological approach used in this paper for enhancing the slew-rate and gain characteristics of two-stage operational amplifiers (op-amps) introduces an auxiliary monitoring circuit, activated exclusively during slewing conditions, aimed at augmenting the op-amp's performance in terms of slew-rate and gain. Simulations conducted on a 0.18 µm technology platform demonstrate noteworthy outcomes, including a DC gain of 74 dB, a bandwidth of 160 MHz, and a slew-rate of 26.8 v/us. These results are achieved while accommodating a load capacitance of 1.75 pF and consuming a mere 362 uW of amplifier power at a supply voltage of 1.8 volts. This approach addresses the inherent challenge of balancing performance with power efficiency in contemporary portable systems, particularly in the context of low-power and low-voltage applications [17]. This paper has designed a folded cascode using TSMC 0.18µm CMOS technology by using improved recycling folded cascode architecture which results in less settling error percentage [18]. This article deals with a low power consumption high speed folded cascode opamp which uses a switching circuit to minimize the power consumption. It provides a gain of 51dB and a 0.996 V output dynamic range [19]. The paper explains the small signal analysis of the folded cascode Opamp. It discusses about the placements of poles and zeros and derives an equation for minimum settling time (MST)[20].

3. METHODOLOGY

Operational amplifiers (op-amps) are versatile devices widely employed in electronic circuits for a myriad of applications. These devices, being direct coupled, have the capability to amplify both DC and AC signals without necessitating coupling capacitors. Characterized by their exceptionally high open-loop voltage gain, op-amps can magnify minute input signals into significant output voltages. Originally devised for mathematical operations such as summing amplifiers, integrators, differentiators, and various mathematical functions, op amps serve both linear and nonlinear applications.

Packaged as single integrated circuits, op-amps offer convenience and ease of use, seamlessly integrating into electronic designs. Their inclusion simplifies circuit design by reducing reliance on extensive external components. Furthermore, op amps find utility beyond basic amplification tasks; they serve as filters, comparators, oscillators, and voltage regulators, showcasing their versatility and indispensability in modern electronics.

3.1 Functional block diagram

For a better understanding of the working of a folded cascode, let’s divide the circuit into 4 blocks.

1)Tail current
2)Differential pair
3)Current source
4)Wide swing cascode current mirror

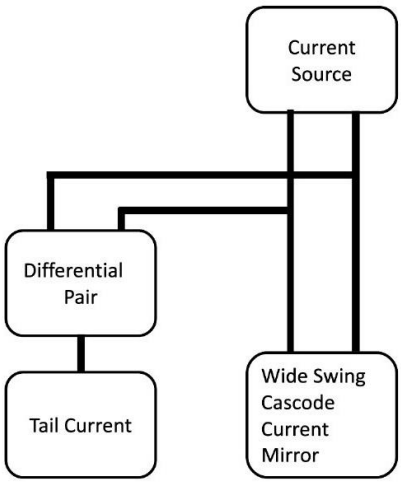

Fig. 1 Block Diagram

1) Tail Current: The tail current block provides a constant bias current to ensure proper operation of the differential pair transistors. The current in transistor M1 is mirrored in transistor M12 as shown in Fig. 5, which establishes and maintains the constant bias current. By providing a stable bias current, the tail current block ensures that the differential pair operates in its linear region, allowing for accurate amplification of input signals.
2) Differential Pair: The differential pair amplifies the volt age difference between its two input terminals; the differential pair has two transistors M0 and M11 as shown in Fig. 5 responds to input signals applied to the gates of each transistor. The current flowing through the MOSFETs depends on the gate-source voltage Vgs, where an increase in Vgs leads to an increase in current and vice versa. Differential input voltage applied to the gates modulates the currents in the transistors, causing one transistor's current to increase while the other's decreases, resulting in amplification of the differential voltage. The differential pair's amplification of the voltage difference forms the core function of the op-amp, providing gain to input signals.
3) Current Source: The current source block, consisting of transistors M17 and M6 as shown in Fig. 5, supplies a high current that is later distributed to other parts of the circuit. Transistors M17 and M6 facilitate the highest current f low in the circuit. This current is subsequently split and is directed to the cascode current mirror and differential pair for their operation. By providing a high current source, this block ensures that other components of the op-amp receive adequate current for their respective operations, maintaining proper functionality and performance.
4) Wide Swing Cascode Mirror: A current mirror is a fundamental circuit widely utilized for duplicating current in various applications. However, it comes with inherent limitations, including a confined output voltage range and imperfect current mirroring. A significant challenge in a simple current mirror shown in Fig. 2 arises from the unequal drain source voltages (vds1 ≈ vds2) across transistors, even when their gate-source voltages (vg1 = vg2) are matched. This discrepancy in VDS values poses difficulties in achieving precise current replication. To address these issues, the cascode current mirror configuration is often preferred. In a simple current mirror, equal vgs between transistors do not ensure equal vds. In contrast, a cascode current mirror tackles this problem by biasing one end of the MOS transistors, ensuring the drain voltage on one transistor is equal to that on the other. This guarantees more accurate current mirroring, overcoming the limitations of the simple current mirror. Additionally, the cascode design enhances the output voltage swing, making it advantageous in applications where precise current replication and a broader output voltage range are essential.

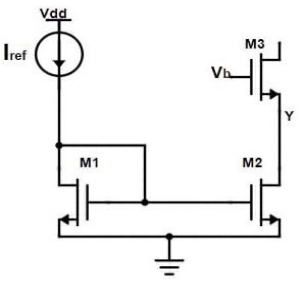

Fig. 2 Current mirror

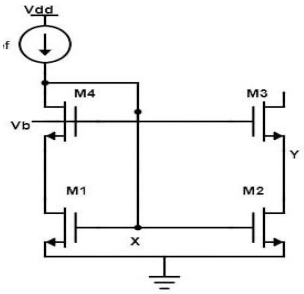

Fig. 3 Wide swing cascode current mirror

In Fig 3. The wide swing cascode current mirror is chosen the output resistance has been improved and has same input impedance. It also has less biasing voltage and gives a high wide swing compared to other current mirror. In summary, the cascode current mirror is utilized to alleviate channel length modulation effects and enhance the output voltage, resulting in improved performance compared to a simple current mirror.

3.2 Equations

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \qquad (1)$$

$$V_{ov} = V_{gs} - V_{th} \qquad (2)$$

Equation (1) helps to determine the W/L ratio of the MOSFET according to the voltage conditions of that MOSFET. Equation (2) is to calculate the overdrive voltage to ensure the region of operation of the MOSFETs. In the previous analysis of MOSFETs, we calculated the aspect ratios of transistors, with specific attention to ensuring the devices operate in the saturation region (region 2). For transistors M2 and M5, the initially calculated aspect ratio was 3u.

From the small signal analysis of the circuit, the following can be derived,

$$Rout = (gm_5 * ro_5 * ro_8) \parallel \left(gm_4 * ro_4 * (ro_6 \parallel ro_{11})\right) \qquad (3)$$

$$gm = gm_0 = gm_{11} \qquad (4)$$

Where, gm refers to the transconductance of the MOSFET and ro refers to the resistance offered by the MOSFET.
The total gain of the circuit is given by,

$$Gain = gm * Rout \qquad (5)$$

By fluctuating the W/L ratios of the MOSFET such as to increase the resistance of MOSFETS M5, M8, M4, M6, M11

and transconductance of M0 and M11 the gain of the circuit can be increased to desired value.

Table. 1 Transistor sizes

Transistor Name	W/L Ratio	W/L Ratio Modified
PMOS (M17 , M6)	22.5µ/180n	14.5µ/180n
PMOS (M7 , M4)	15µ/180n	4.5µ/180n
NMOS (M2 , M5)	14µ/180n	1.5µ/180n
NMOS (M14 , M3)	3µ/180n	1µ/180n
NMOS (M0 , M11)	13µ/180n	36.5µ/1µ
NMOS (M1 , M12)	3µ/180n	23µ/1µ

However, as we observed these MOS devices operating in region 3, we adjusted enhance their performance in the saturation region. To achieve this, we increased the aspect ratio of M2 and M5 to 4u. This modification allowed the MOS devices to transition into region 2. Throughout this process, we made strategic assumptions aligned with MOS FET operation and characteristics, prioritizing the focus on saturation behavior. The careful selection of aspect ratios for the MOS devices was crucial to meet our design specifications and ensure optimal performance in the saturation region.

3.3 Initial Schematic Design

Using the ratios provided in Table 3.1, a folded cascode op-amp was designed with a biasing voltage. The goal was to increase the gain of the op-amp, utilizing the formula Gain = gm * rout. Initially, an attempt was made to enhance the rout by halving the W/L ratio of the current source and wide swing cascode current mirror (comprising M17, M6, M7, M4, M2, M5, M14, M3).

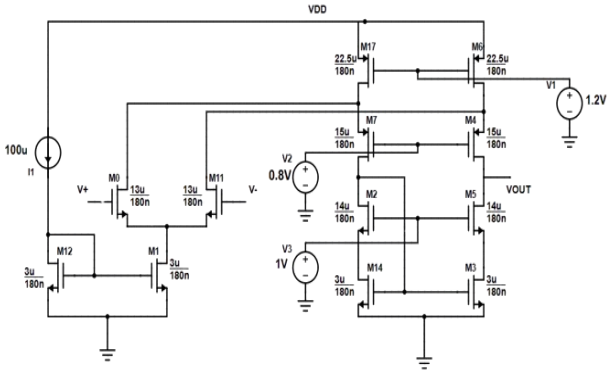

Fig. 4 Folded Cascode Op-amp

The reduction in MOSFET size effectively increased the channel length, leading to higher output resistance. In the context of the gain equation (Gain = gm * rout), this increase in rout contributed to a higher overall gain. The circuit was re-designed which increased the output resistance (rout). This modification led to a noticeable improvement in gain, and interestingly, a shift in the phase of the circuit was observed.

3.4 Final Schematic design

To achieve a further increase in gain, a strategic approach involved enhancing the trans-conductance (gm) of the circuit. This was accomplished by adjusting the W/L ratios of the Differential pair and Tail Current MOSFETs (M0, M11, M1, M12) while maintaining the specified ratios. The key modification included increasing both the width (W) and length (L) parameters of these MOSFETs. Simultaneously, a refinement in the biasing technique was implemented. The biasing voltage source was replaced with a MOSFET biasing configuration.

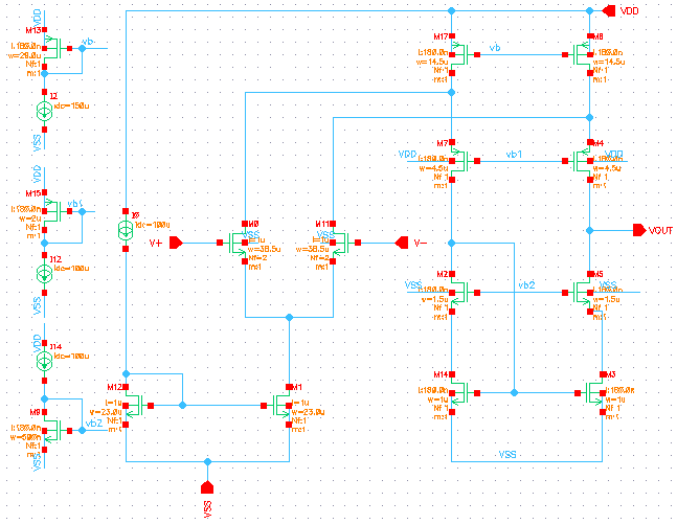

Fig. 5 Final Folded cascode

4. IMPLEMENTATION

4.1 Final architecture

The circuit shown in Fig. 6 represents the single stage folded cascode amplifier, a configuration frequently employed in integrated circuit design due to its advantageous characteristics such as high gain, wide bandwidth, and enhanced input impedance. At the heart of the circuit lies the operational amplifier (op-amp). Here several sources are given for its working. idc serves as the reference current for the circuit used for establishing the amplifier's biasing conditions and ensuring stability. The input signals are provided through the inverting terminal(V+) and non-inverting terminals(V-). The V+ receives a DC voltage along with AC voltage at a specific frequency. The non-inverting terminal of the op-amp is connected to a only DC voltage source. The vout terminal denotes the output voltage of the op-amp, representing an amplified rendition of the input signal. It is linked to a 1pF capacitor, which aids in stabilizing the output voltage and filtering out high-frequency noise or disturbances. This comprehensive setup allows for meticulous analysis, including DC, AC, and transient using the Cadence tool. Various types

of analyses have been conducted on this test circuit, including DC, AC, transient, and output checked, to verify its functionality and performance.

4.2 Simulation using cadence

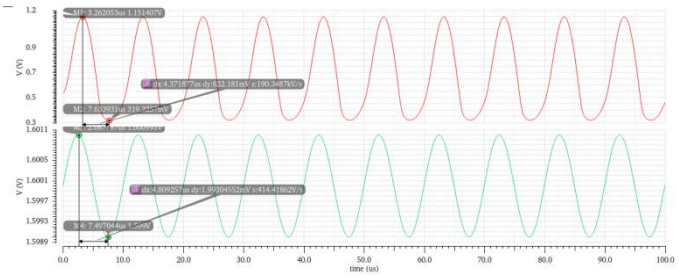

Fig. 6 Transient Analysis of folded cascode

1) Transient Analysis: Transient analysis is conducted to verify the gain acquired in AC analysis. In transient analysis, the circuit is simulated over a period that allows us to observe its dynamic behavior in response to time-varying signals or transient events.

During transient analysis measure the gain of the circuit by comparing the input and output voltages over time. By observing the waveform of the input signal and the corresponding output signal, we can calculate the gain as the ratio of the output voltage to the input voltage at each point.

$$Gain = 20log_{10}\left(\frac{V_{in}}{V_{out}}\right)dB \qquad (6)$$

The gain calculated from transient analysis using equation (4.1) and should ideally match the gain obtained from AC analysis. In AC analysis, the gain is determined by applying small signal variations around the circuit's operating point and analyzing the frequency response of the amplifier. This gain value represents the amplifier's behavior over a range of frequencies. If the gain calculated from transient analysis closely matches the gain from AC analysis, it indicates that the circuit operates consistently across different scenarios(analysis) and effectively amplifies input signals with minimal distortion. This ensures that the gain remains consistent between transient and AC analyses. This can validate the accuracy of simulation results and confirm the circuit's performance meets the given design specifications. Any huge difference in the gain values may indicate issues in the circuit.

2) DC Analysis: DC analysis is a fundamental technique used in Cadence and other circuit simulation tools. Unlike transient analysis, which focuses on dynamic behavior over time, DC analysis examines the steady-state behavior of the circuit, considering only the DC components of the input signals. This analysis is essential for establishing the operating conditions, biasing points, and overall stability of the circuit. In the context of our circuit simulation, DC analysis was utilized to verify whether all components, especially MOSFETs, remain in saturation mode throughout operation. MOSFETs operating in saturation mode are crucial for proper circuit functionality and performance. By subjecting the circuit to DC analysis, we can ensure that MOSFETs remain in saturation region under different operating conditions, such as varying input voltages. By verifying the saturation of MOSFETs through DC analysis, we can confirm that the circuit operates as intended and meets design specifications. Any deviations from saturation mode can be identified and addressed during the design phase.

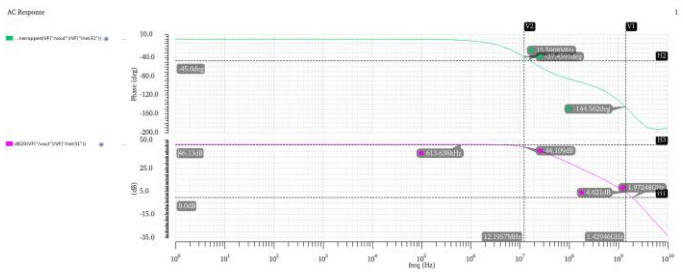

Fig. 7 Initial gain-phase analysis

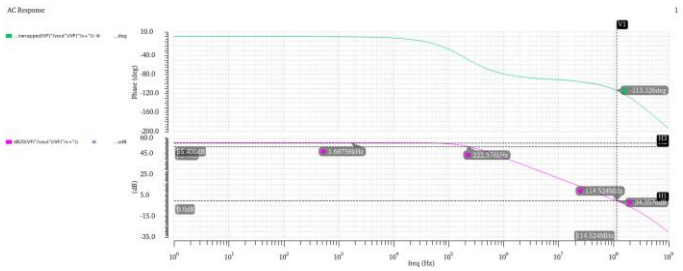

Fig. 8 Final Gain-Phase analysis by increasing gm and Rout

3) AC Analysis: In Cadence, as in most electronic de sign automation (EDA) tools, AC analysis plays a crucial role in analyzing the frequency response of electronic circuits.AC analysis assesses how circuits react to sinusoidal signals at various frequencies, in contrast to transient analysis, which looks at circuit response over time. In the following topic, AC analysis is being used to find out the proper frequency response of the system. By calculating the DC operating points, it analyzes the circuit from a start to stop frequency. Consequently, this process allows us to determine the gain, phase, and bandwidth of the circuit. To determine the gain, look for the frequency at which the magnitude reaches its maximum value, corresponding to the circuit's mid-band gain. This gain is often expressed in decibels (dB). Phase margin, which indicates the stability of the amplifier, can be calculated from the phase response. It is the difference between the phase at the frequency where gain crosses 0 dB (unity gain) and-180 degrees. Bandwidth can be obtained by directly reading it from the Bode plot or deriving it from the frequency response data. Taking the determined specifications enables the optimization of the folded cascode for the specific applications for the designer. Analyzing the circuit's behavior in the frequency domain allows designers to adjust component values, compensation techniques, and biasing schemes to meet

specific performance requirements while maintaining stability across the targeted operating frequency range. This examination is essential for the design of folded cascode amplifiers in contemporary analog integrated circuits, ensuring their dependability and effectiveness in various applications.

5. RESULT ANALYSIS

PVT analysis is an analytical method for examining a circuit to understand how it performs when the parameters of Process (P), Voltage (V), and Temperature (T) are varied. These factors determine the reliability and performance of the given circuit. Variations in the process refer to the changes that can occur during the manufacturing stage of the semiconductor, leading to deviations in the power and speed given circuit. Variations in the process refer to the changes that can occur during the manufacturing stage of the semiconductor, leading to deviations in the power and speed of the circuit. Voltage variation refers to the change in the main supply voltage (VDD), which affects the power consumption and behavior of the circuit. Temperature variation leads to changes in transistor mobility, threshold voltage, and leakage current, affecting the reliability of the circuits.

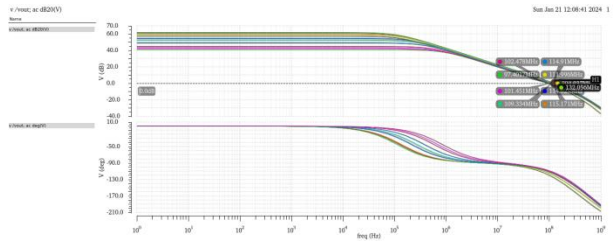

Fig. 9 Final Gain-Phase analysis

There are 5 process corners to be checked. FF – Fast-Fast: FF refers to the best-case condition where the transistors are assumed to be the fastest, with the lowest threshold voltage and shortest channel length. FS - Fast Slow: FS refers to more realistic conditions where some transistors are fast while others are slow. SS – Slow-Slow: SS refers to the worst-case scenario where transistors are assumed to have the slowest performance due to the largest threshold voltage and longest channel length. SF – Slow-Fast: SF refers to a case where some transistors are slow, and others are fast. This corner helps analyze the behavior of the design when there are mixed process variations, such as slower transistors and faster transistors. TT - Typical: Here, the process parameters, supply voltage, and temperature are set to their typical values to check the functionality of the circuit under normal conditions.

Table. 2 Simulated results table

Design Parameter	Specification	Simulated Value
DC gain	50 dB	55.40dB
Phase Margin	60 deg.	66.87 deg.
Slew Rate	100V/µs	100V/µs
Bandwidth(-3dB)	200KHz	222kHz

6. CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

This project has successfully implemented a fully functional folded cascade operational amplifier circuit with 180 nm technology. The design process was designed with provided specifications, involving a keen understanding of how alterations to different circuit components could influence various performance parameters. During the simulation phase, the circuit was simulated with various analyses covering DC, AC, and transient analysis.

Although time constraints led to the deferral of the layout portion of the circuit design, the comprehensive analysis presented in this paper focused on the design of a folded cascode amplifier using 180nm CMOS technology. This involved initially designing a single-stage cascode op-amp, and subsequently, enhancing it into a high-gain folded-cascode op amp with improved output resistance, leading to higher gain compared to a normal cascode circuit. The simulations were conducted using Cadence, showcasing the circuit's ability to achieve high gain and a substantial phase margin, bandwidth, and another parameter.

The proposed folded cascode op-amp structure, designed for various applications, demonstrated high DC gain and slew rate, along with a large output voltage swing. The optimization of MOS components proved challenging but was successfully achieved through careful simulation analysis. The op-amp met all specified requirements as mentioned in Table II.

In conclusion, the folded cascode op-amp offers improved DC gain, enhanced bandwidth (BW), and a better phase margin. This work contributes valuable insights into the overall operation and advantages of the folded-cascode circuit, ad dressing limitations of previously prevented architectures and paving the way for further advancements in amplifier design.

6.2 Future Scope

There is significant potential for improvement in the circuit's performance. Future efforts could focus on optimizing the design to achieve enhanced output swing, higher gain, and other desirable characteristics. Additionally, exploring alternative configurations and topologies may provide insights into further refining the amplifier's capabilities. This amplifier holds promise for diverse applications such as serving as a buffer or a crucial component in a Digital-to-Analog Converter (DAC) and in LDOs. In an LDO, a folded cascode configuration serves as the error amplifier, providing high precision and stability for constant voltage regulation. It compares input voltage error with a reference voltage, amplifies the error signal, and adjusts the output voltage accordingly through the pass transistor(s). As we progress, addressing these future considerations will undoubtedly contribute to the ongoing evolution and refinement of the circuit for broader applications in the field.

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