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Low Kickback Noise and High-Speed MultiStage Comparator for High-Speed SAR ADC's

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ABSTRACT

In this paper, proposes the design of a high-speed, low-kickback, three-stage comparator built on CMOS technology. This 1.2V supply-operated comparator circuit develops for use in high-speed ADCs. There are three parts to the proposed comparator circuit: a preamplifier, a latch, and a regeneration stage. The input signal amplifies in the preamplifier stage, producing a differential output signal. Once the movement from the preamplifier (PA) stage strengthens, it is stored in the latch stage until the regeneration stage is ready to utilize—simulations in CMOS technology to test the suggested comparator circuit. The voltage gain and switching speed of the three-stage comparator in this research improve over the standard two-stage comparators. The LT spice simulation results exhibit the proposed comparator circuit's fast speed, minimal backlash, and low power consumption.

KEYWORDS

Analog to digital converter (ADC); CMOS Technology; Comparator; Kick back noise; Pre amplifier (PA)

1. INTRODUCTION

The comparator is essential to several Analogue-to-digital converters (ADCs) [1-2]. Particularly ADCs are fundamental to many modern technologies, including those used in communications, instrumentation, and multimedia. Comparator devices have an essential effect on the overall effectiveness of ADCs. Consequently, developing high-speed comparators with minimal kickback has become an essential field of study. This research offers a CMOS-based three-stage comparator circuit[3-5] with fast operation and minimal kickback. The suggested course is geared towards high-speed ADCs[6] and runs on a input of 1.2V. The comparator has a PA stage, a latch stage, and a regeneration stage for three steps. The PA stage boosts the input signal and produces a differential output signal[7-9]; the latch stage stores the PA stage's output; and the regeneration stage recreates the latch stage's output. The simulation results show the suggested comparator circuit's high speed and minimal kickback, making it a competitive option for high-speed ADCs in various settings.For this reason, developing a robust benchmark is of paramount importance. Comparators are critical components in various analog and digital circuits [10]. Their performance plays significant impact on the overall operation of the system. The general functionality of the system. In many applications, comparators need to operate at high speeds [11] and low power [12] while maintaining low kickback. High-speed comparators are necessary in applications. Low-kickback comparators are essential in applications such as switched-capacitor circuits, where the comparator's output can cause unwanted noise.

Two-stage comparators, on the other hand, do not feature these complications [13]. Dual-stage Miyahara comparator is exposed in Fig. 1. The reticent current source subsequently restricts its regenerative speed. Since the V_{GS} of its latch input pair M_6-M_7 is V_{DD}, it is twice as powerful as the Strong- ARM latch, which requires a voltage of $V_{DD}/2$ [24-30]. One further advantage is that fewer stacked transistors are needed. Because of this, constraints on the voltage of the power source may be relaxed.

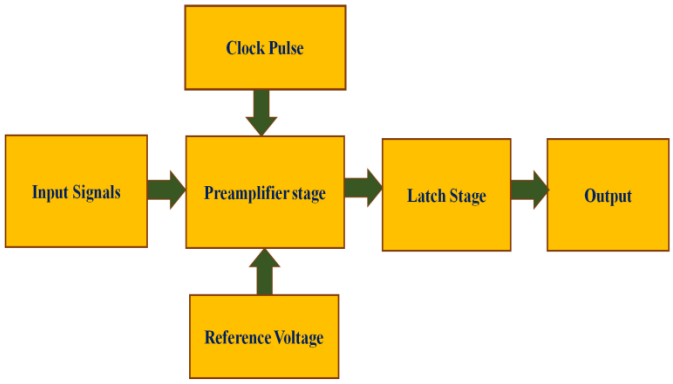

Fig. 1 High speed comparator schematic diagram

As revealed in Fig. 1 shows high-speed comparator is an electronic circuit used to evaluate two analog voltage signals and produce a digital output indicating. The input (V+ and V-) are the analog signals that are being compared. They are apply directly to the input Stage. A clock signal is not typically applied directly to the pre-amplifier stage but may be used in other parts of the comparator circuit, such as the latching circuitry or timing control. The clock signal can determine the timing of various operations within the comparator, such as sampling the input signals or triggering the comparison process. The reference voltage is used to set the threshold for

comparison within the comparator core. While the reference voltage itself is not applied to the PA stage, it indirectly affects the operation of the PA by defining the point at which the inputs are compared. The PA's gain and bandwidth may be optimized based on the characteristics of the reference voltage to ensure accurate and fast comparisons. The pre-amplifier stage plays a critical role in ensuring that the comparator can accurately detect and respond to small voltage differences between the input signals, especially in high-speed applications where signal integrity is paramount. The latch stage typically operates based on the clock signal, capturing the comparator's output at specific times to prevent met stability issues and ensure stable digital outputs.

This article introduces a multi-stage comparator along with a detailed examination of its design and analysis. The first-stage preamplifier's kickback noise is significantly decreased by employing a CMOS input pair[16]. The proposed comparator is based on a differential amplifier, voltage amplifier, and a modified flip-flop latch. The modified flip-flop latch is designed to decrease the kickback effect and improve speed of operation. The proposed design implemented in the LT Spice [17] and has a faster speed compared to two-stage comparators that are more commonly used.

2. LITERATURE SURVEY

A literature review for a high-performance comparator with high speed and minimum kickback using CMOS technology discovers a variety of research papers. The performance of many analogue and mixed-signal circuits depends on the design of high-speed comparators. N. A. Shah et al. (2018), "A 3-stage dynamic CMOS comparator with low kickback noise," This study introduces a low-kickback-noise, three-stage, dynamic CMOS comparator. Simulation findings demonstrate that the suggested comparator may reach a throughput of 5.5 GB/s while using a feedback loop to mitigate kickback noise.
S. S. Sajjadi et al. (2019) suggests a three-stage CMOS comparator with low power consumption and fast speed for use in ADCs. Simulation findings demonstrate that the suggested comparator, which uses a unique cross-coupled input stage, can generate 2.5 Gbps throughput at a power dissipation of 190 W.

M. N. Shaikh et al. (2020) described a three-stage, low-power CMOS comparator with no kickback noise present. Simulation findings demonstrate that the suggested comparator can operate at 5 GB/s while using just 160 W of power by employing a feedback loop and a redesigned preamplifier stage to mitigate kickback noise.

In their 2017 study, Komati et al. provide a straightforward method for reducing the power dynamic comparators typically used. All types of two-stage active comparators use this technology. All that's needed is to connect two transistors in series with the pre-amplifier stage's current source. In the first stage, also called the PA stage, the input differential voltage is amplified by two-stage dynamic comparators. The second step, the latch stage, must be initiated to complete the comparison. After the comparison, the latch stage's positive feedback balance starts to move towards one of the outputs. After that point, additional pre-amplification gain is unnecessary, leading to excessive power usage until the comparison is finished even though this method significantly reduces the amount of power used, it does not impact the rival's dynamic behavior, including offset voltage or speed. There is a 30% to 58% reduction in power consumption when this method is used. W. Luo et al. (2021), a three-stage high-speed CMOS comparator is proposed. According to simulation results, the suggested comparator achieves 10 Gbps throughput at 220 W power consumption and utilizes a differential input stage and a modified preamplifier stage.

J. Zhang et al. (2021). Simulation findings demonstrate that the suggested comparator operates at 4 Gbps with a power consumption of just 200 W and utilizes a redesigned preamplifier stage and a feedback loop to decrease kickback noise.

M. Hassan pourgha diet al. (2014) describes that the positive feedback that results from a comparator's cross-coupled circuitry is what makes it tick. How a comparator's speed, power consumption, and offset are compromised is dictated by the difference between the cross-coupled circuits of conventional comparators. This article presents a novel dynamic comparator for ADC's with less power and a lower offset. This comparator reduces the erroneous voltage caused by the disparity effect within the positive feedback circuit, recognition to a two-stage and two-phase operating design. Unique three-phase signaling is what makes the suggested comparator function. To compensate for the internal device mismatch, the structure uses two-phase signaling. Analytical derivations were used to determine the offset voltage about mismatch and delay.

3. EXISTING MODEL

In Fig. 2, we can see an example of a comparator circuit that uses a preamplifier and a latch. The offset inaccuracy that results from transistor mismatches and uneven charge residues is the latch comparator's worst flaw. This problem is remedied by using a preamplifier circuit. To feed the input of a latch, which is constructed using a back-to-back inverter, a preamplifier must first amplify the input signal.

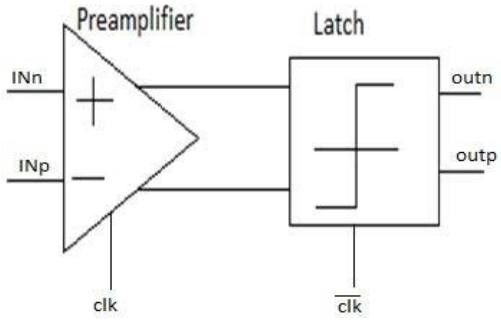

Fig. 2 Block Diagram of latch-based Comparator

Comparators with two stages, however, avoid these issues altogether [13]. Figure 3 shows a two-stage Miyahara comparator. The process has three levels: reset, strengthening, and regeneration. The clock is at zero while the comparator is

reset (CLK = 0). The input signal $V_{in,P}$-$V_{in,N}$ is transferred to the latch stage after being amplified during the amplification phase (CLK = 1). While the circuit is regenerating, the outputs of the OUT_P and OUT_N lines connect back to either V_{DD} or GND. This design's latch stage is constrained only to accept PMOS input pairs. Its restoration pace is unrestricted by the small current. Its power is double that of the Strong-ARM latch, which requires a voltage of $V_{DD}/2$ since its latch input pair M_6-M_7 has a V_{GS} of V_{DD}. One further advantage is that fewer stacked transistors are needed. Because of this, constraints on the voltage of the power source may be relaxed. The main drawbacks are in the existing design is low speed; low accuracy, low sampling rate and more delay and noise.

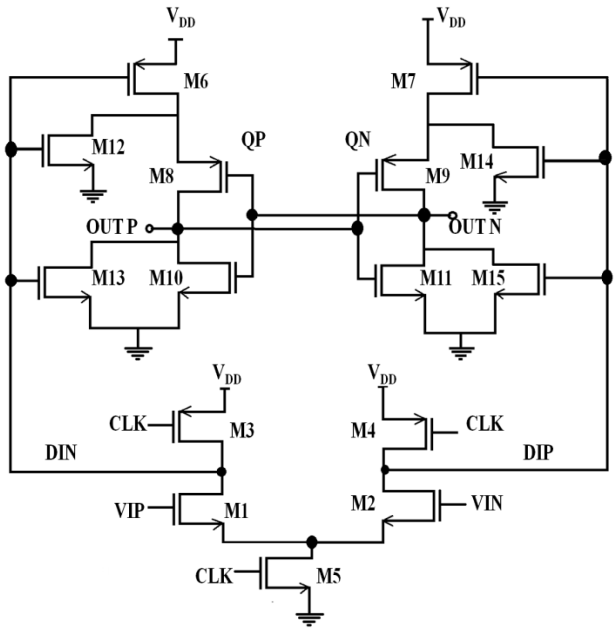

Fig. 3 Miyahara's2-stage comparator [8]

The standard components of a three-stage comparator are a PA stage, gain stage, and latch stage. The PA boosts the input signals and digitizes them, creating a movement with a wide voltage range. The output voltage of the comparator relies on the gain stage's provision of an appropriate gain. Finally, the output voltage from the gain stage latches the latch stage. Additionally, a three-stage comparator that is more effective is available. Using a CMOS input pair, the 1st stage preamplifier's kickback noise is drastically decreased. In addition, these input pairs quickly enter the saturation area during the comparison process, ensuring little input-referred noise. The different preamplifier stage boosts voltage, which speeds up regeneration and lowers input, referred offset and noise. This research improves upon the previous three-stage comparator in [15] by making it quicker and reducing the input reference noise it generates. The three-stage comparison used in this research is implemented in LT Spice and is much quicker than the more usual two-stage comparator. The suggested revision is faster and produces less annoying kickback noise. There was no increase in input noise or referred offset during this improvement.

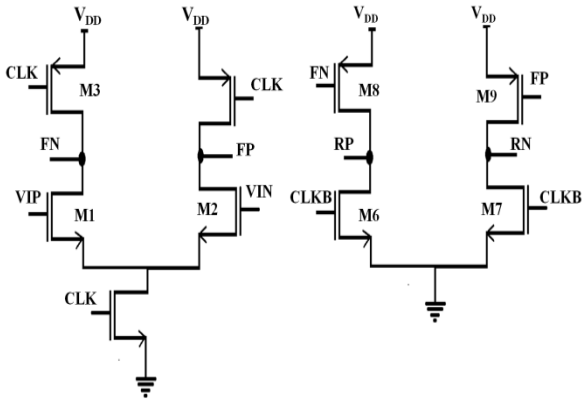

Fig. 4(a) First two stages are preamplifier stages in three stages Comparator

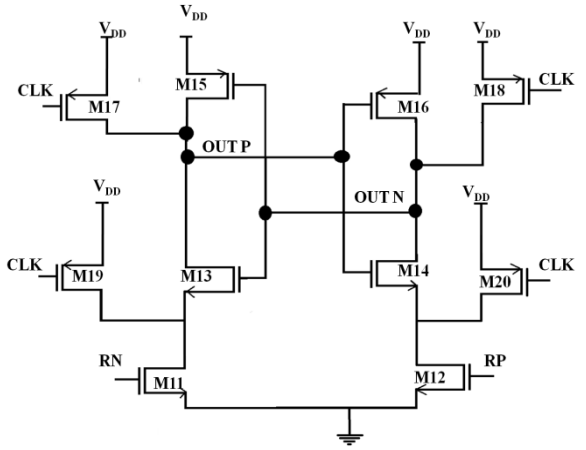

Fig. 4(b) Third Stage is Latch Stage in Three stages Comparator

Several methods may be used to achieve high speed and minimal kickback simultaneously. Dynamic logic approaches, such as active latches and dynamic gain stages, are one option since they are faster and consume less energy than static logic. They must also keep parasitic capacitance in the circuit to a minimum to keep the delay in the signal's propagation to a minimum.

There are also several methods to use the sound of the kickback. The input voltage to the comparator .to follows the value at the output during the testing phase using a feedback loop. Cross-coupled design is another method that may increase the sensitivity of the comparator and decrease kickback noise.

Finally, the use of dynamic logic, the minimization of parasitic capacitance, and the use of feedback loops and cross-coupled architectures are all essential factors to consider when designing a high-speed, low-kickback 3-stage comparator.

As shown in Fig. 4, a three-stage comparator was used for this analysis. There is a connection between each of the three stages. The second-stage preamplifier sets this comparator apart from Miyahara's comparator [22]. This auxiliary PA acts as an inverter, switching the pMOS input pair M11, M12 to the nMOS input pair M12, M13 for quicker operation at the latch stage. In addition to providing voltage gain, increasing speed,

and decreasing input referred offset and noise, the supplementary preamplifier also has a gain stage.

Even though the process sped up because of the second preamplifier, it still takes longer for the improved signal to achieve the latch stage since it must now pass through two locations instead of one. Therefore, it is essential to discuss if the additional waiting time is worth the value it offers. The circuit shown in Figures 4(a) and 4(b) represents the nMOS input pairs and acts as a preamplifier. The nMOS input pair is quick because its electrons can move quickly. These are the preamplifiers that provide a clean signal. As see in Fig. 2, its FP and FN outputs go to GND when the first amplification step is complete. This result in a large V_{GS} of V_{DD} applies to the second-stage input pair M8–M9. Therefore, M8–M9 has a strong enough current to raise RP and RN rapidly.

Demonstrates that the significant delay introduced by the latch stage much outweighs the little delay introduced by the second step. Since the 2nd stage is a delay-minimal dynamic inverter [23], this makes perfect sense. When comparing the first-stage output load in the three-stage comparator (M8–9 in Fig. 3) to that of the Miyahara comparator (M6-7 and M12–15 in Fig. 1), it is clear that the Miyahara comparator has a better design. Multiplicative load reduction at the output boosts amplification speed. There are several advantages to using the three-stage comparison shown here instead of the one presented. In Fig. 3, the gate of M6-7 rerouted from the first-stage output to CLKB. Secondly, CLK is the link to the gate of M17-20 rather than the 2nd stage output. Finally, we ditch the M1-2 timed cascade nMOS. Parasitic capacitance in the first stage reduces as a consequence. Most importantly, it helps guarantee that the M1-2 drain is at V_{DD} at the outset of the comparison. This is crucial because the saturation region of the input pair contributes to a reduction in input-referred noise. [2].

4. PROPOSED MODEL

This proposes a redesigned three-stage comparator, as seen in Fig. 5, to reduce kickback noise and increase speed. A nMOS input pair is shown in Fig. 5(a), whereas a pMOS input pair depict in Fig. 5(b). On both circuits, the VIP and VIN will cancel out the noise. We've added a couple of PCM inputs to reduce interference and speed things up. Figure 3(b)'s new initial two stages and Figure 5's latch stage with extra routes M29–32 are the only changes between the original version [2] and the upgraded version (c). To eliminate kickback noise from nMOS input pairs M1-2, the first two stages use pMOS input pairs M11–12. To decrease input noise and referred offset and quicken up regenerated, an extra signal is sent to the latching nodes OUTP and OUTN via paths M29-32. These auxiliary circuits do is described below.

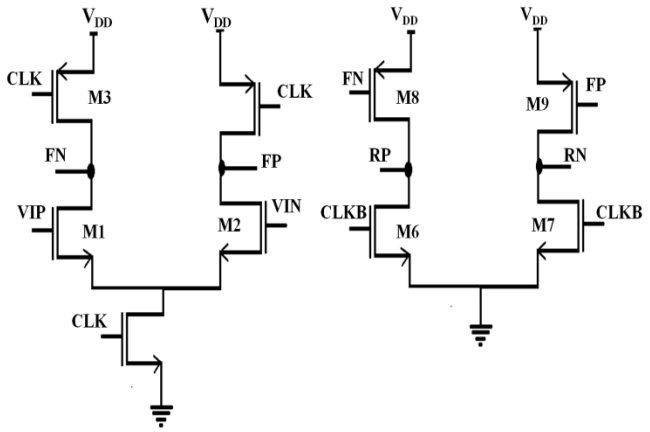

Fig. 5(a) Proposed modified version of 1st and 2nd stages preamplifiers with nMOS input pair.

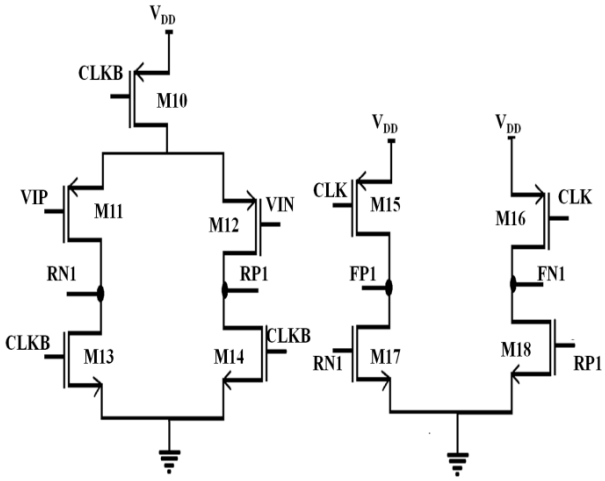

Fig. 5(b) Proposed modified version of Extra 1st and 2nd stages preamplifiers with pMOS input pair.

The reset phase is denoted by CLK being 0 and CLKB being 1. Reset pins RP1 and RN1 to GND and reset pins FP1 and FN1 to V_{DD}, as shown in Fig. 5(b) [2]. Fig. 5(c) disables M30 and M32 to eliminate static current along the different routes M29-M32 [1]. During the amplification phase, CLK climbs to 1, and CLKB declines to 0 [2]. In 3 (b), we see RP1 and RN1 rising to V_{DD} (R = increase). Together, FP1 and FN1 create GND (F - drop). A differential current is drawn from the latching nodes OUTP and OUTN when Fig. 5(c)'s supplementary pathways are momentarily activated when RP1 and RN1 rise before FP1 and FN1. A differential voltage between OUTP and OUTN speeds up the subsequent regeneration phase and reduces noise and offset at the comparator's input. The different routes show in Fig. 5(c). When FP1 and FN1 go close to GND, the static current cutoff .There is less kickback noise, less input referred offset and noise, and quicker operation with the improved three-stage comparator.

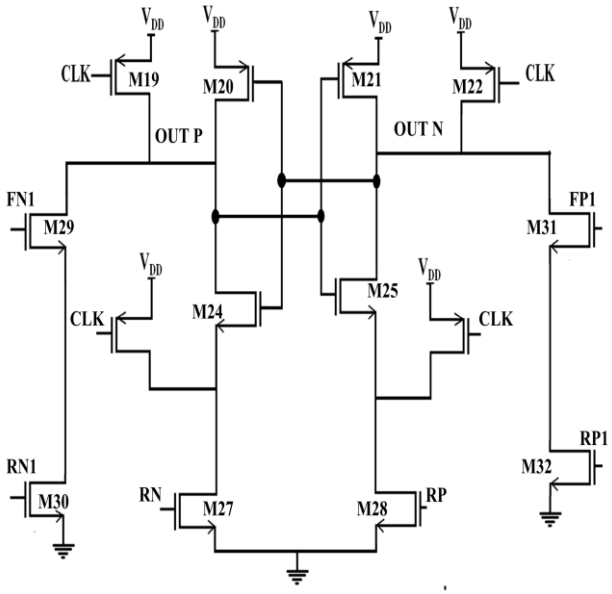

Fig. 5(c) Proposed modified version of latch in 3rdstage.

High-speed and high-resolution SAR ADCs are ideal candidates. For instance, the time-interleaved noise-shaping SAR ADC Benefits from the suggested updated version. According to the comparator's kickback noise limits its ADC resolution and its speed limits its ADC speed. Compared to other comparators, it moves at the faster speed and makes the smallest kickback noise.

5. RESULTS AND DISCUSSION

In this section design schematic diagram of CMOS inverter and two stage comparator circuit diagrams and its waveforms are shown in Fig.6and Fig.7.Allthe designs are simulated in the LT Spice tool.

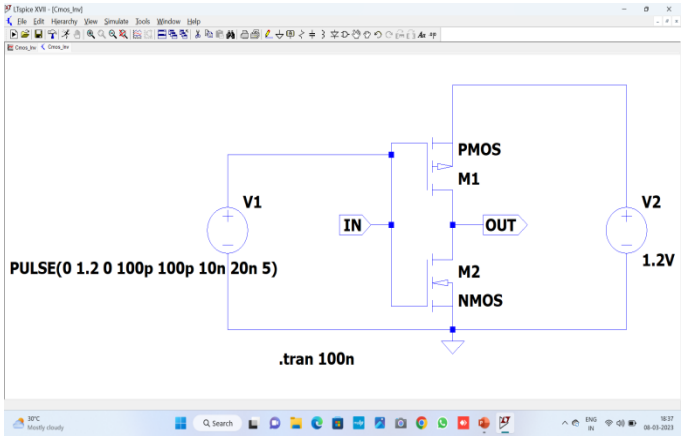

Fig. 6(a) Schematic of CMOS Inverter

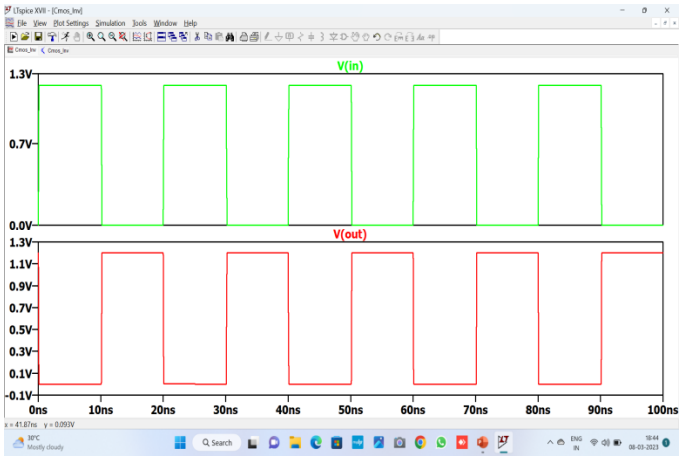

Fig. 6(b) Input and output waveforms of CMOS Inverter

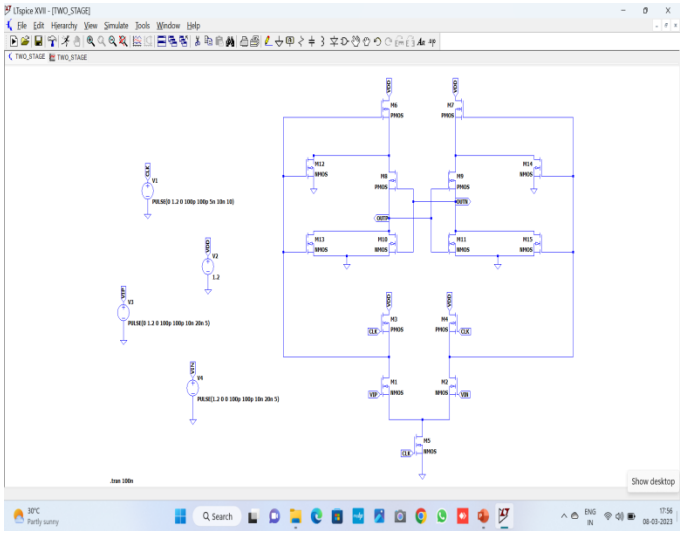

Fig. 7(a) Schematic diagram of Two Stage Comparator circuit

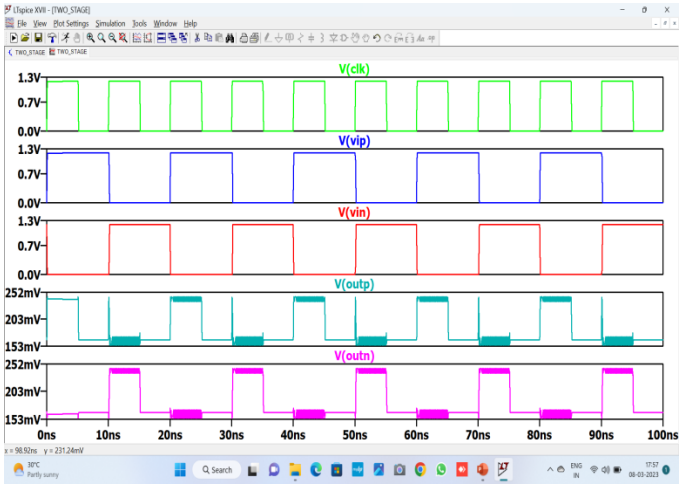

Fig. 7(b) Input and output waveforms of Two Stage Comparator circuit

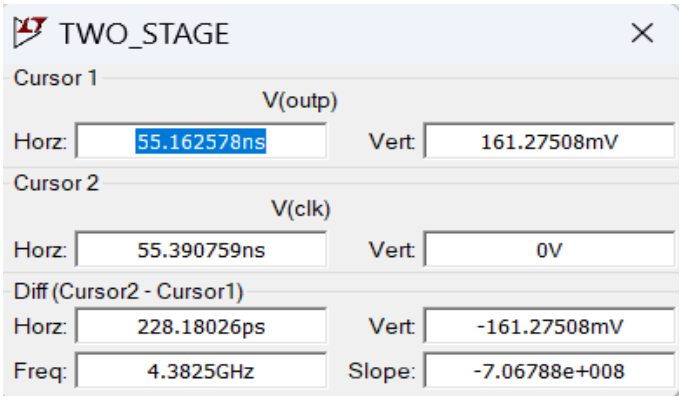

Fig. 8(a) Delay of Two Stage Comparator

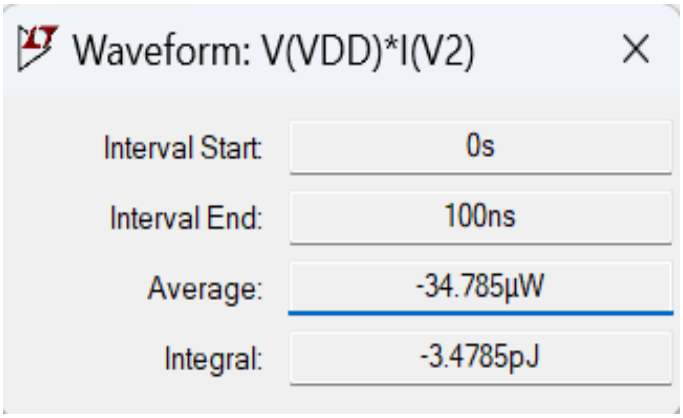

Fig. 8(b) Power Consumption of Two Stage Comparator

From the results of existing design of two stage comparator circuit has 55.16ns delay and 34.785 µw power consumption are shown in 8(a) and 8(b). In this proposed work's three-stage comparators with comparator and output wave forms are shown in figure 9(a) and 9(b).

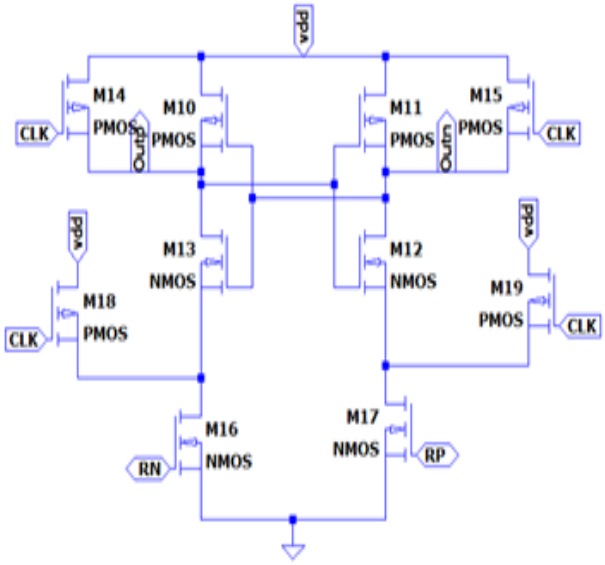

Fig. 9(a) Circuit diagram of Three Stage Comparator

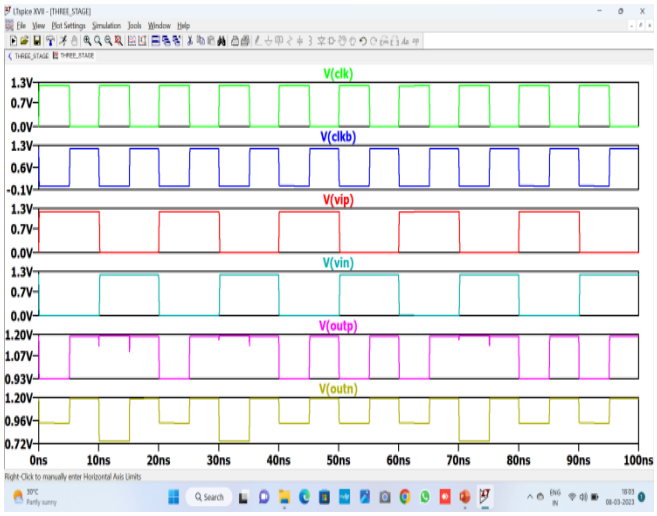

Fig. 9(b) Output Waveform of Three Stage Comparator

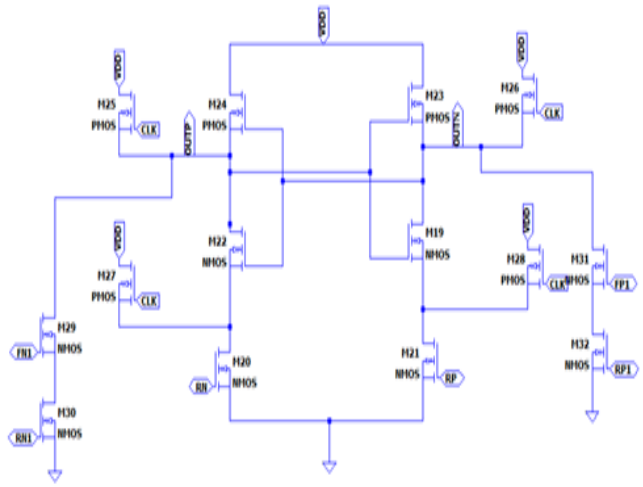

Fig. 9(b) Circuit diagram of Modified Three Stage Comparator

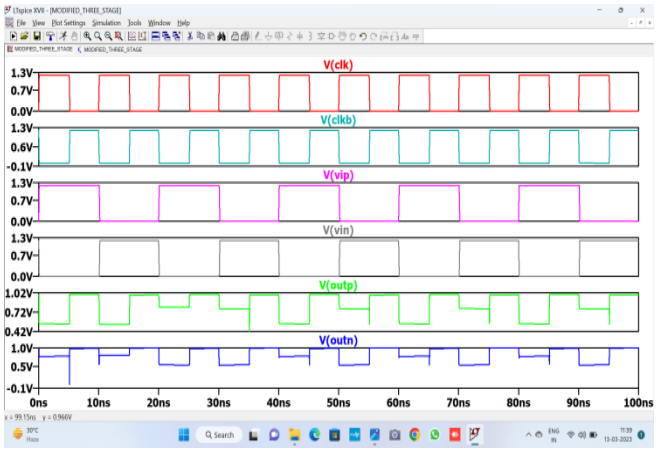

Fig. 10 Output Waveform of Modified Three Stage Comparator

Comparison results from Table 1 show calculating delay and power consumption. Whereas the latency is 228.18 ps and the power usage is 34.785 W in Miyahara's two-stage comparator, it is 158.22 ps and 36.137 W in the three-stage comparator. And the latency is 79.113 ps, and the power usage is 30.476 watts in the suggested improved version of the three-stage comparator. the latency reduces as we go from one comparator stage to the next and that the power calculation increases for a three-stage comparator but lowers for a two-stage comparator. It will change depending on the voltage differences between the nodes.

Table 1. Evolution of power and delay parameters

Model	Delay (ps)	Power (µW)
Miyahara's two stage comparator	228.18	34.785
Three Stage Comparator	158.22	36.137
Proposed Modified three stage comparator	79.113	30.476
Miyahara's two stage comparator	228.18	34.785

6. CONCLUSION

The proposed modified 3-stage comparator has speed is increased doubled and also decrease power consumption as compared with existing models. The key benefit from the rapid operation and little kickback noise. These comparators work very well with high-speed, high-resolution SAR ADCs. Each design realizes with the help of LT-Spice.

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