International Journal of Microsystems and IoT

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Published online: 22 January 2024.

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Design and Implementation of Multiplier Accumulator Unit Using Rounding Based Approximation

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ABSTRACT

This paper presents an analysis of the design of a programmable gain amplifier (PGA) based on an instrumentation amplifier. The instrumentation amplifier can be implemented in different ways, including the Single Op amp IA, 2 Op-amp INA, 3 Op-amp INA, Switched Capacitor Instrumentation amplifier (SCIA), Current Feedback Instrumentation amplifier (CFIA), Current Mirror Instrumentation amplifier (CMIA), and others. By adding switches or a multiplexer (Mux) to the amplifier, a precision programmable gain instrumentation amplifier (PG-IA) can be created. The literature suggests various approaches for enhancing the performance parameters of a PGINA, and this study aims to bring together and evaluate these approaches on a unified platform. In this research, an extensive examination of multiple instrumentation amplifier topologies has been carried out, and these topologies have been categorized based on their distinctive characteristics.

1. INTRODUCTION

The batteries in the latest portable devices (e.g. laptops, tabs, mobiles…) is limited size and the number of multimedia applications are growing with an exponential power rate, hence high energy efficient DSP architectures are most requirement. Several DSP applications need low power consumption and outstanding performance for real-time signal processing, as well as fast-speed and high-throughput multiplier-accumulator (MAC) units. Since MAC is essentially refined by redundant use of addition and multiplication, the speediness of the addition and multiplication arithmetic decides the execution speediness and execution of the whole count. The DSP cores in the smart devices will perform huge number of multimedia applications for the human benefits, where the hum intervention is very limited; hence the designs should be very energy efficiency with minimum loss of quality. This can be achieved at many design/modeling levels such as device, logic, circuit, algorithmic and architectural level. Hence the research should be in a direction such that the design of adders and multipliers should include approximate computation logics, and to bring the trade-off between many VLSI parameters. Multiplication operation is a blessing in a few components of an advanced framework or figuring gadget, most remarkably in signal interaction, designs, and logical calculation. The algorithmic programming that Booth developed may have a significant positive impact on the pattern of signed binary multiplication. Energy reduction is one of the critical necessities of any electronic device, incredibly portable like sophisticated mobile phones, tablets, and other gadgets. Achieving this decrease with the bare minimum of execution (speed punishment) is highly desired.

These typical devices' primary components for recognizing various multimedia demands are called DSP cores. In these DSP systems, the ALU unit is the central processing unit, and multiplication operations have the optimal distribution among all other ALU jobs. Therefore, increasing the multiplier's speed and power/energy efficiency becomes crucial for enhancing CPU performance. Because of this fact, we may employ approximations to boost efficiency and speed. To start, humans have a limited ability to take information presented to them in the form of a picture or video. The accuracy of the arithmetic operation is not fundamental to the usage of the system in many contexts, not only those involving video and image processing. Having access to the approximation register gives the designer more flexibility in terms of trading off precision for speed, power for efficiency, and so on. Power proficiency and high performance of a system can be acquired by approximate processing, and it can likewise diminish the complexity in design. In the most common DSP architectures, the multiplier is a crucial piece of hardware. Commonplace DSP uses where a multiplier has a major role Because of their small size, today's electronic devices use a lot of energy. Given the complexity of multipliers and their high clock rate, this helps reduce the time it takes to perform a multiplication.

An adder, multiplier, and accumulator make up MAC. In this activity, we multiply the two numbers together and add the product to a counter. A MAC unit comprises of amount of the past progressive items. The plan of a performance high 64-bit Multiplier-Accumulator (MAC) is carried out utilizing Verilog HDL. When partial items are created, they should be ordered and supplemented in a deliberate way with extraordinarily less deferral.

It is possible to estimate the ALUs at the circuit, reasoning, and engineering stages of design. The estimation might be performed utilizing various strategies.

Many multipliers reported in the literature, reducing the complexity of the design and the number of components [1–4], using an approximation compressor to accumulate sets of partial outcomes yields reduced latency and energy consumption [5–9]. The use of approximation adders for accurately computing the addition of the final two sets following a compressor is achieved by splitting the process into two stages [10]. The inaccuracy in an approximation multiplier was reduced by using bitwise AND-OR gates to calculate insignificant parts, as described in [11]. In [12], we see a multiplier implementation that uses a signature with just two bits. This research article is organized into five sections below. Section 2 has the discussion over the literature survey of the work. Similarly, section 3 discusses basic MAC unit and basic RoBA multipliers, and the modified RoBA multiplier and MAC processes. The design approach of all the units discussed here. In section 4, the implementation process of all the blocks in Verilog HDL, simulation results and the Synthesis reports of the designs discussed. The comparisons among the different multiply along with proposed multiplier discussed. The final section represents conclusion.

2. LITERATURE SURVAY

Broken Multiplier (BMA) technique was employed in the design of an approximate adder and multiplier explained in [13]. With the use of BAM approximation design in [13] a conventional altered Booth Multiplier is modified assigned binary approximate multiplier presented in [14]. The approximate multiplier design has low power and less area when compared to a systematic Booth multiplier. Approximate multipliers have an approximate buildings block that leads to reduce power consumption around 31.8%–45.4% when compared to the normal multiplier designs. A Pipelined processor implementation using an approximate signed multiplier of 32-bit design presented in [15]. This design has an error of nearly 14%, and the design exhibits higher speed compared to full adder-based Wallace tree multiplier. An error-resistant multiplier, which appraised the inaccurate outcome by separating the multiplication operation into one accurate and one inaccurate part discussed in [18]. This design exhibits a 50% reduction in power consumption when applied to a 12-bit multiplier. In the publication [16], two approximation compressors were developed and evaluated using a conventional DADDA Multiplier. Many approximate multipliers which were used earlier are more reliant on either changing the design or intricacy decrease of a particular precise multiplier. An approximate Wallace tree multiplier using with an incorrect counter 4:2, has been presented in [19]. Here, additionally an auto error correction unit recommended correcting the results. To design a larger size of multipliers, this incorrect WTM can be in an array structure. As in [17], we proposed doing the approximate multiplication through simple operation. The extensive literature over this topic can be read from the papers [20-26]. The novelty of this paper with the other literature papers is that the approach may be same for signed and unsigned numbers, but this design is faster than other designs and techniques. The suggested architecture has a unified multiplier that can handle both signed and unsigned operations. This technique has a low mistake rate. This project aims to develop and execute a low-power MAC block using a block-enabling approach to achieve substantial power savings. This work initiated with the design of 1-bit MAC unit along with power, area, and delay optimization algorithms, later its extended to the N-bit MAC. Control logic is designed to enable the pipelined stages at an appropriate time, consequently, reduces the power usage. High speed adder cells with low gate count along with low power included in the design process.

CNN for Security in Computer Vision and Multimedia

Le Cun et al. achieved pioneering research by using CNN in conjunction with the back propagation method to recognize handwritten postal codes, resulting in a significant level of accuracy. Due to advancements in machine functioning faster, particularly in graphics processing units, In [4] developed a sophisticated and deep CNN called AlexNet. This design won the ILSVRC2012. Some minor modifications desire to be made to AlexNet's training resources and network layout. They then developed a pre-trained CNN called CaffeNet, which is based on the Caffe framework and is the benchmark model. The power of deep models has been further enhanced by the widespread use of fine-tuning; a popular technique rooted in transfer learning. Some layers in a base network that have already been trained can be used to train a new job more efficiently by refinement. Within the field of multimedia security, several methods employ CNN for steganalysis [6]–[8] and image forensics. There were positive results reported in [6] for a deep model that used CNN for structural analysis. Subsequently, Pibre et al. [7] conducted a study on the "structure" of convolutional neural networks (CNNs) and determined the optimal CNN model through extensive experimentation. CNN had much better performance than older steganography methods when using a previously used confidential key to insert information. Nevertheless, the efficacy of their model when employing a random private key for each embedding in a practical scenario was inferior to that of conventional methods relying on manually designed features. They presented a CNN deep model for detecting hidden information in images using JPEG-domain steganography. This approach differs from the traditional method of analyzing the spatial domain of the image [8]. The CNN architecture was enhanced by incorporating the concept of JPEG-phase awareness. Tuama et al. [4] employed a combination of a high-pass filter and CNN for source camera identification. This approach allowed for the automatic extraction of features and simultaneous learning for classification.

Bondi et al. [5] recently used a convolutional neural network (CNN) to automatically extract distinctive camera model characteristics. They then trained a support vector machine (SVM) for classification. This approach surpasses prior approaches in analyzing tiny color picture patches, and its characteristics show a solid potential to generalize. Bondi et al.

[6] used these profound characteristics to create an iterative clustering approach that effectively addresses the problem of detecting and pinpointing picture manipulation. Previous CNN-based approaches for multimedia security, as shown in references [2], [3], [6], [8], including current approaches [4], often use a preliminary layer in the deep model that is somewhat arbitrary, either fixed or limited. This layer typically consists of one or more HPF and remains unchanged, making it non-trainable during training. In [6] and [8] used a high-pass filter (HPF) to isolate the remaining noise of an input picture at the lowermost part of their network.

In [2] CNN used an initial set filter level that takes an image as input and produces the residual of its median filtering as output. This effectively carries out nonlinear high-pass filtering. In [3] developed a limited filter layer for global picture alteration recognition. In this layer, the filter kernel's center is set to -1, while the sum of the other components is set to +1. The first layer must acquire a collection of high-pass prediction error filters within a specific limitation. The primary concept behind this is presumed to have a high frequency while reducing the input picture's semantic information (mostly believed to have a low frequency). As RGB pictures are input, our study's first layer has a 3-D filtering set instead of 2D linear convolutional kernels. The 3D convolutional filters may be trained without limitations, making them adaptable. Our tests and visualization show that such filters readily bring out valuable and unique features from the data we received for our classification task. While revising this publication, we discovered a new study called Stats Net that similarly utilizes CNN to differentiate between CG pictures and NIs [5]. In Section V–H, we look at our method in detail, including both personal and numeric comparisons. Our method is better than Stats Net in several areas, especially on the tough Columbia dataset including network layout, design, and test performance. Pan et al. [11] recommended a process that takes advantage of fractal dimensions to identify the difference in color perception between photos and computer-generated images. A technique to differentiate between computer-generated and genuinely captured human faces was suggested by Nguyen et al. [12]. Pattern noise is the basis of the technique developed in [14] and [15] devised a method using demosaicking and chromatic aberration traces. Analyzing demonstration traces using threshold-based classification is the approach put forth by Gallagher et al. [16]. The features of CFA iteration and image response variation noise are used. A method was suggested by Peng and Zhou [17]. While using this method, the SVM classifier achieved a classification accuracy of up to 99.5%. This method shows promising results even when dealing with additive noise and JPEG compression. A CNN classifier and noise from sensor patterns are the ingredients in the recipe that Yao et al. [18] laid forth. When tested on a picture dataset of 1800 CG and PG images, the method achieved 100% accuracy. This research compares existing methods to distinguish between computer-generated (CG) images and photos (PG) using characteristics associated with the image-gathering process. A combined method using both texture interpolation and local patch statistical features was suggested by Sankar et al. [19]. It was possible to use both wavelet-based features and complex pattern noise data by Conotter and Cordin [20] as a possible method. A method combining the ResNet-50 model with CNNs was suggested in [21]. 4850 computer-generated and photographically generated images was used to assess this method. A classification accuracy of 97% was reached using the approach.

The feature length is 2048, which is considerable. Two investigations were conducted by Holmes et al. [22] that used the human visual system. To classify images as computer-generated (CG) or photographically generated (PG), they engaged 250 people from Amazon's Mechanical Turk online workforce. Researchers have shown that trained experts, rather than amateurs, should examine the images to improve classification accuracy. Farid et al. [23] presented a statistical model for images using the first four-order wavelet coefficient statistics in different sub bands. To implement this method, we computed 216 features and then used a support vector machine classifier to determine whether the image was CG or PG. Research using a dataset of 40,000 PG pictures and 6,000 CG images has confirmed of 71% classification accuracy. In the discrete Fourier transform area, Cui et al. [24], a method that depends on comparable properties. This method reportedly attained an accuracy rate of 94% on the Columbia photo dataset. A total of 780 characteristics are obtained by computing the statistical moments of the 1-D and 2-D characteristic functions. In the next step, the SVM classifier is fed these characteristics [25–29]. The method of increasing feature selection further reduces the number of attributes to no more than 390. Applying this method to the Columbia photo dataset yields a subpar classification accuracy of 88%. Bo et al. [30] introduced a technique that uses SVM classifiers and Benford's law. This method uses a 54-length feature vector, which is computationally efficient. This method achieves a classification accuracy of 91.6% on a dataset that includes 2400 CG and 2400 PG images.

3. PROPOSED DESIGN

In this chapter, basic MAC approach modified MAC approach, basic ROBA and modified ROBA multiplication techniques and the design processes discussed.
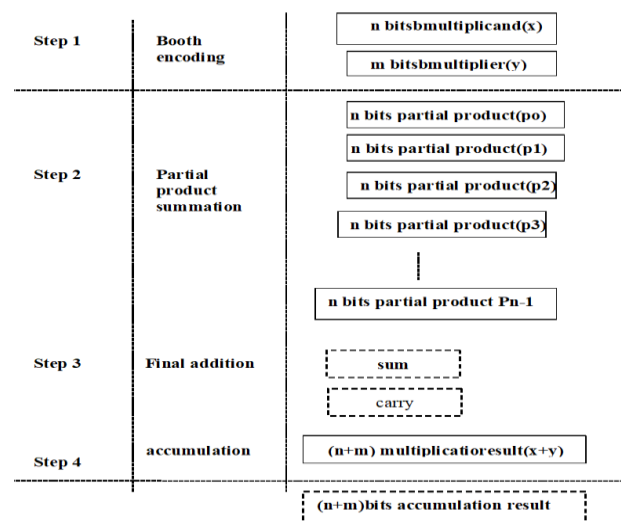
3.1 Basic MAC approach

Fig. 1 Basic arithmetic steps of multiplication and accumulation.

In Fig. 1, we can see the fundamental procedures for adding and multiplying. The action of a multiplier is split into three distinct phases. The radix-2 Booth encoding is a method that employs the multiplicand X and multiplier Y to generate a sample product. Additionally, there's the option of using either an adder array or partial product compression technique to merge all the partial products and convert them into a format that consists of the total and carry. You get the multiplication result when you add the total and the carry. A MAC has four stages, as shown in Figure 1 (which depicts the operational processes) when the procedure to aggregate the multiplied outcomes is considered.
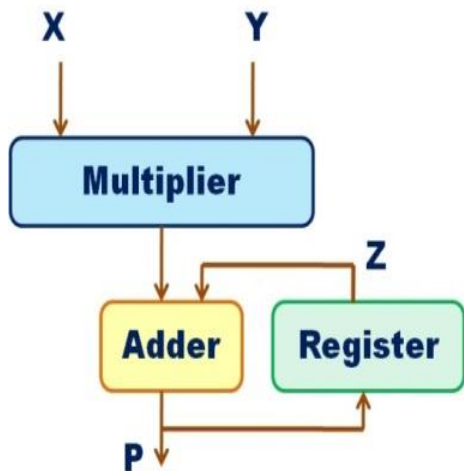
.

Fig. 2. Standard MAC Hardware Architecture

The figure provided illustrates the overall hardware design of this MAC. The multiplication process is performed by multiplying the input multiplier X with the multiplicand Y. This is appended to the prior product Z as the accumulation step [27].

The binary number 2's complement of N-bit 2 is stated as,
$X = -2^{N-1} x_{N-1} + \sum_{(i=0,n-2)} x_i 2^i \quad x_i \in 0,1$

$$(1)$$

To use Booth's technique with a radix-2, express (1) in base-4 redundant sign digit form.
$X = \sum_{(I=0,N/2-1)} d_i 4^i$

$$(2)$$

$D_i = -2x_{2i+1} + x_{2i} + x_{2i} - 1$

$$(3)$$

If we apply (2), multiplication is represented as

$X \times Y = \sum_{(i=0,(N/2)-1)} d_i 2^{2i}$ $\qquad (4)$

With these equations, the fore-mentioned multiplication–accumulation results is expressed as
$P = X + Y + Z = \sum_{(i=0,(N/2)-1)} d_i 2^i + \sum_{(i=0,(2N-1))} z_i 2^i$ $\qquad (5)$

The two factors on the opposite side of Equation (5) are computed separately, and their sum is the result. The architecture provided by (5) is the standard design in the MAC domain.

3.2 Proposed MAC approach

The three-stage modified MAC approach, first shown in Figure 1, is now offered in Figure 3. Here are two modifications: first, the accumulation is now integrated into the adding partial products process, and second, though it is not explicitly indicated, the final addition process of the third step is only sometimes done. Step 3 may be skipped until the result for the final accumulation is needed since the result from step 2 is utilised for accumulation instead of the one from step 3. The proposed MAC's layout is shown in Figure 4. The (n+1) bit partial product was generated from the n-bit MAC inputs X and Y using the Booth encoder. Not only can the nth carry save adder and accumulator do partial product and save additions, but they can also execute accumulation. By adding and carrying the lowest bits of the sum, the n-bit variables S, C, and Z are produced as the result. These three values are returned for the subsequent accumulation. To get the result, P [2n-1: n], the terms S and C are added to the previously created term P[n-1:0].

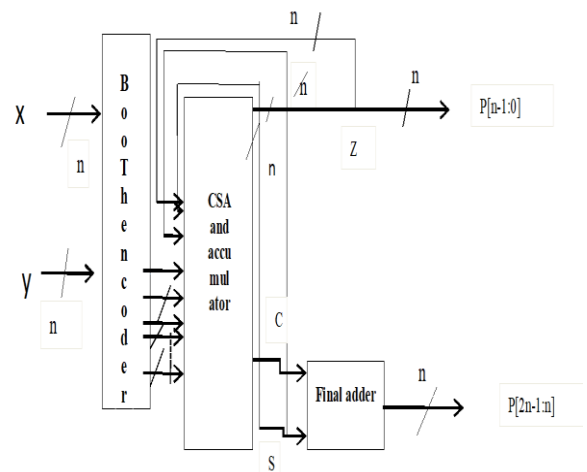**Fig.3.** Proposed multiplication-accumulation operation

Fig.4. Proposed MAC architecture

3.3 Basic Round Based Approximate Multiplier:

Multiplication can be done using shifters, adder, and a subtractor as shown in figure 5. The output of the multiplier changes with the inputs X and Y. This multiplier gives the precise results only for the positive numbers as the rounded values of negative numbers are not in the form of 2n. Therefore, before doing multiplication need to eradicate the sign and then perform the multiplication. After performing the multiplication, the sign should be given to the output based on the input. Multiplication of two input numbers X and Y with the Rounding Based Approximate concept is expressed as is explain here [28].

$$X*Y = (Xr-X)*(Yr-Y) +(Xr*Y) +(Yr*X) -(Xr*Yr) \quad (6)$$

Where Xr and Yr are the rounded nearest power of two of inputs X and Y. The terms $(Xr*Y)$, $(Yr*X)$ and $(Xr*Yr)$ are achieved with the shift logic. The terms $(Xr-X)$ and $(Yr-Y)$ represent rounding error terms of X and Y, these terms can be ignored if X and Y efficiently rounded. Hence, the above equation is approximated as

$$X*Y \approx (Xr*Y) +(X*Yr) -(Xr*Yr) \quad (7)$$

Sign Detector: This is the first block to identify the sign of the inputs and provide sign for the output as for mentioned. If the MSB of the input is '0', it will treat as a positive number, if it is '1', then input will treat as negative integer.
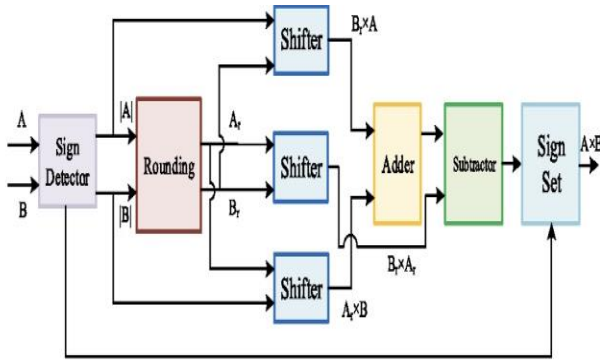

Fig. 5 Basic ROBA

Rounding block: It will perform the rounding of the inputs to nearest power of two value.
Shifter: Multiplication terms, Xr*Y, X*Yr, and Xr*Yr are performed through logical shift operation.
Adder: generates the sum result $(Xr*Y) +(X*Yr)$.
Subtracter: Finds the subtraction of adder and shifter terms, $(Xr*Y) +(X*Yr)-(Xr*Yr)$.
Sign Set: To provide the sign to the output result.

3.4 Modified ROBA

In the above existing method, the term Xr*Yr, suffers from the large error as both X and Y rounded the power of two, and $X*Y \approx (Xr*Y)$ or $(X*Yr)$ will provide high accuracy over the

previous discussed term. If we consider all the terms for multiplication, it leads to an increase in both computational accuracy and design complexity. Hence to bring the trade of between both the parameters, four multiplication terms need to be considered and implemented separately to use as the requirement.
$X*Y = (Xr*Yr)$; $X*Y=(Xr*Y)$; $X*Y=[(Xr*Y) +(Yr*X)]/2$; $X*Y=(Xr*Y) +(Yr*X)- (Xr*Yr)$
The technique shown in figure 5 should be modified in such a way to generate these terms.

3.4.1 Implementation of Proposed MAC with proposed ROBA technique

High-speed multiplication using parallel counters is accomplished via a modified version of the booth method. This partial product generator uses the modified booth method for radix 2 to produce partial products. Instead of shifting and adding for each multiplier term column and multiplying by 1 or 0, multiply every other column by -1, -2, or 0. First, multiply the partial product aligned with the third column by 2, then multiply the product aligned with the least significant bit by -1 to multiply by 7.As a result, the circuit's latency in propagation, complexity, and power consumption have all decreased. Skipping zero rows is feasible using booth multiplication. The modified-Booth encoder circuit in Fig. 7 conserves transient signal power using SPST. A detector regulates this approach. One of the two operands is used by the detecting unit to determine whether the booth encoder is computed redundantly.
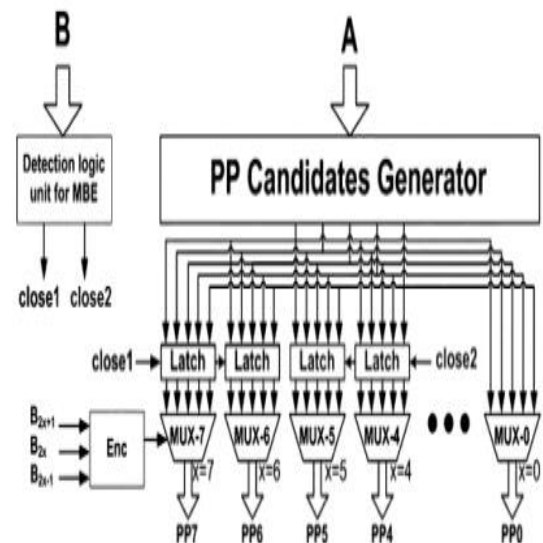

Fig.6 SPST equipped modified Booth encoder

In Figure 6 shows an SPST-enabled version of the booth encoder. The PP generator makes five possible partial products: (2X-X), (X-0), (2X), and (2X-2). Then, they'll make a call based on operand Y's encoded results from both booths. This partial product generator uses the modified booth method for radix 2 to produce partial products. Each group of bits is sent to multiplier group, for each group one partial product is
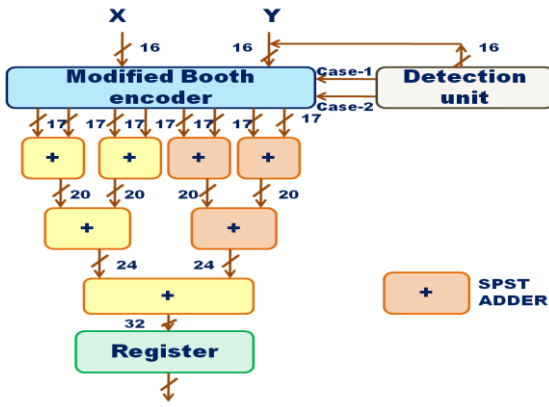
generated.

Fig.7 Proposed high performance low power equipped adder.
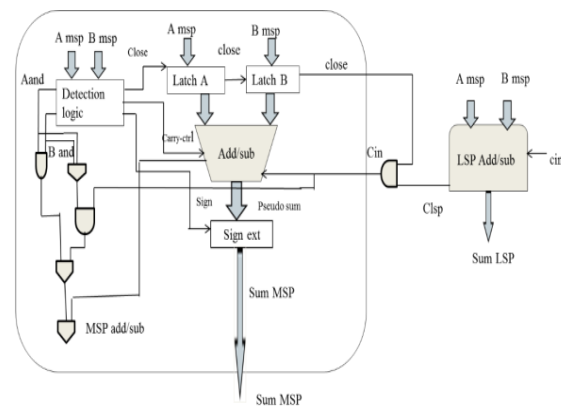

Fig.8 Low power adder/subtractor adopting SPST

A SPST-based adder/subtractor with 16 bits is seen in Figure 8. The 8th and 9th bits of a 16-bit adder/subtractor are split off to form the MSP and LSP, respectively, in this implementation. AND gates are used to implement latches, which are used to regulate the MSP's input data. When the MSP is required, its input data remains unchanged; when it is not, its input data becomes zeros to prevent unnecessary switching power usage.
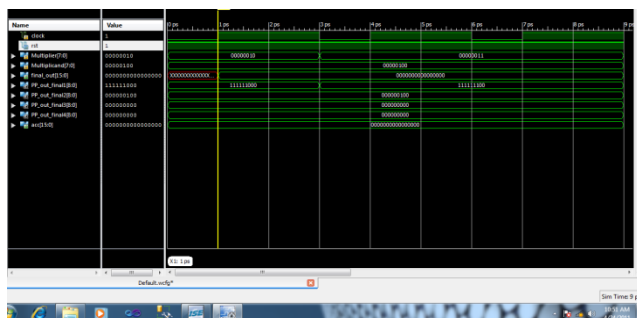
4. RESULT AND DISCUSSION
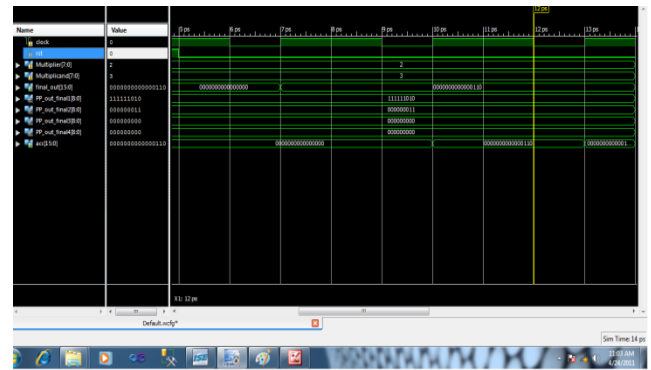

Fig.9 Case(i):MAC CSA Output with reset=1
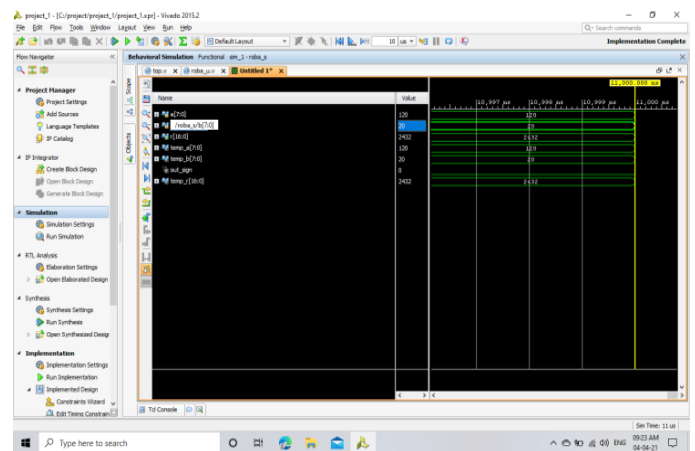

Fig.10 Case(ii):MAC with CSA output with reset 0.

Fig.11 Modified RoBA Multiplier result.
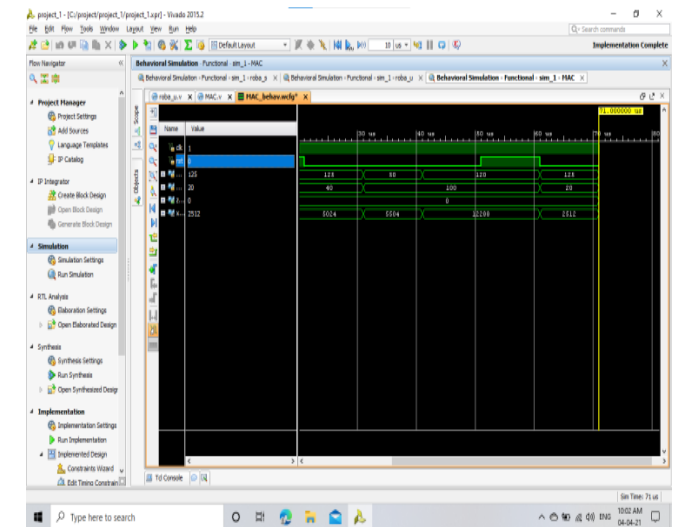

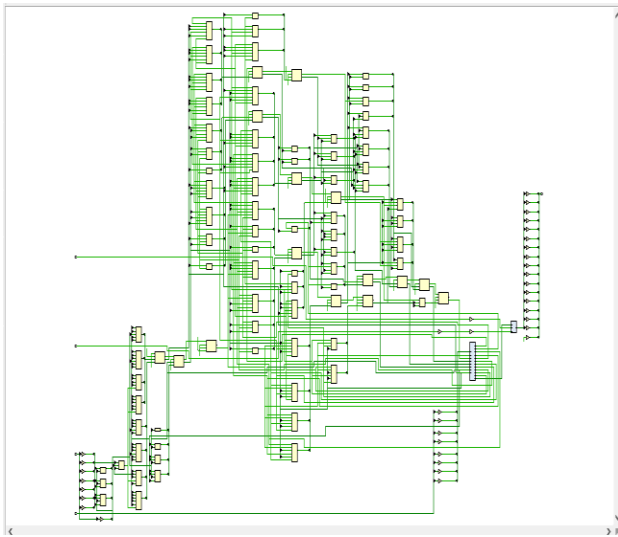**Fig.12** Multiplier accumulator unit using ROBA.

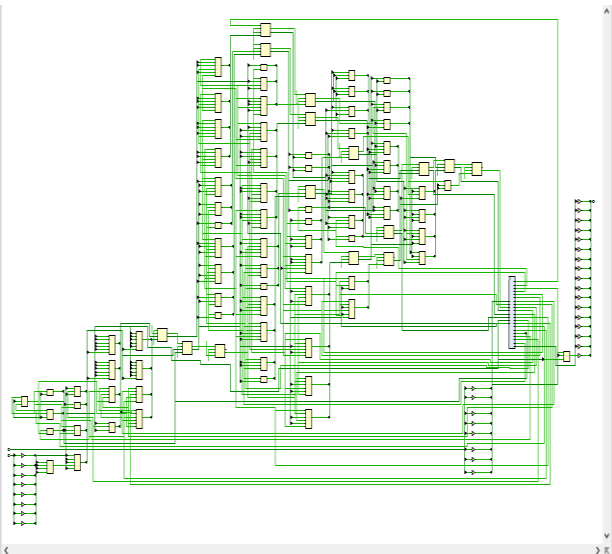**Fig.13** Modified RoBA Multiplier RTL schematic

Fig.14 MAC with Modified RoBA technique RTL schematic.

Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, and Figure 14, shows MAC CSA Output with reset=1, MAC with CSA output with reset 0, Modified RoBA Multiplier result, Multiplier accumulator unit using ROBA, Modified RoBA Multiplier RTL schematic, MAC with Modified RoBA technique RTL schematic respectively.

Table 1 and Table 2 shows Synthesis report, and Comparison with existing design parameters.

Table 1: Synthesis report

mac1 Project Status			
Project File:	mac1.ise	Current State:	Synthesized
Module Name:	top_tst	• Errors:	No Errors
Target Device:	xc3s500e-4fg320	• Warnings:	22 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

mac1 Partition Summary		[-]
No partition information was found.		

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	1182	4656	25%
Number of Slice Flip Flops	678	9312	7%
Number of 4 input LUTs	1863	9312	20%
Number of bonded IOBs	1	232	0%
Number of BRAMs	4	20	20%
Number of GCLKs	2	24	8%

Table 2: Comparison with existing design parameters

Types of Multipliers	Max Output time (ns)	Delay (ns)	Power (mW)	Area (IOBs)	Error Rate
VedicMultiplier [5]	21.470	2.63	17.58	50	1
Baugh-Wooley [7]	15.181	1.59	17.42	40	1
RoBAMultiplier [28]	10.436	1.14	9.21	33	1
Modified RoBA multiplier	9.21	0.84	1.1	26	1
MAC [27]	5.8	1.21	2.7	16	1
MAC withRoBA multiplier	15.22	1.97	10.4	42	1
MAC with modified RoBA multiplier	7.252	1.05	5.37	36	0.29

5. CONCLUSION

This paper, the basic ROBA multiplier is modified and is used in the implementation process of modified MAC process. Since the SPST technique, modified booth algorithms and approximate rounding terms generation process has been simplified and reduce the complex terms and number of transition signals, the accuracy and the power consumptions values are improved in the MAC with modified ROBA than the MAC with ROBA implementation. The modified MAC reduced to three stages of execution from four stages of execution. Nearly 50% delay and power reduced in the proposed design designs.

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