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Performance Analysis of PCT in JPEG-XR/HD Image Compression System

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ABSTRACT

This paper presents the importance of photo core transform in JPEG-XR/HD. Integer based coding technology is the basis for JPEG-XR/HD image compression system. Different HDR formats can be compressed by using this JPEG-XR/HD system. The main advantage of pulse core transform (PCT) is high compression efficiency and less computational complexity. In JPEG-XR/HD image compression system the photo core transform has been used to perform compression. Photo core transform based JPEG-XR/HD image compression system has been widely used in real time embedded applications. Adder, shifter and parallel multiplier circuits are used for the implementation of this photo core transform. By using this design it is possible to reduce the area, cost and power consumption.

KEYWORDS

unified Photo core transform Enhanced dynamic range Entropy encoder JPEG-XR/HD Integer coding

1. INTRODUCTION

With rapid increase of different imaging applications, the memory requirements of digital images are growing at an exponential rate. Translation from image pixels into frequency domain by using two-stage lapped biorthogonal transform (LBT) in JPEG-XR/HD. Two key components are there in the LBT transform, they are the photo overlap transform (POT) and the photo core transform (PCT). Among the two transforms, the PCT is very much needed, where as the POT is optional. The PCT is the main functional block in JPEG-XR/HD, hence many researchers have proposed different architectures for the hardware implementations [1-4]. LBT and advanced Huffman coding are used in the JPEG-XR/HD[2]. By JPEG-XR better quality images are produced than JPEG at the same bit rate, and implements both lossless and lossy compression. To decompose an image into frequency components PCT is helpful. This process is similar to discrete cosine transform (DCT) of JPEG. During conversion process a'macroblock'which is in rectangular area is processed by PCT [5-7]. To reduce block noise, which occurs around macro block boundaries, Photo overlap transform (POT) is used with PCT [8][9] using different architectures. JPEG-XR/HD is very much useful when compared to JPEG2000 for High definition (HD) photo and High dynamic range(HDR).By using JPEG-XR/HD less computational cost is possible[10-14]. Many applications such as telemetry, telemedicine and multimedia signal processing JPEG-XR is widely used. The main functional block of JPEG-XR/HD compression standard is PCT shown in figure 1. JPEG-XR processing methodology is same as conventional image compression techniques but PCT makes this technique a better choice for image compression [15-16].

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Fig. 1 Block Diagram of JPEG-XR/HD System

JPEG-XR/HD proved to be an efficient method for industry requirements upon comparing with JPEG and JPEG2000. The JPEG-XR/HD has a capability of getting high throughput for encoding millions of samples [17], [18].

The remaining part of the paper is outlined as follows: The architecture of Photo core transform proposed depicted in Section II. Implementation of the algorithm covered in Section III. Section IV explores the results on applying the JPEG-XR/HD codec using Xilinx ISE to input images. Finally, section V covers the work conclusion.

2. EVOLUTION OF PHOTO CORE TRANSFORM

JPEG-XR/HD constructed by Lapped bi-orthogonal transform (LBT) .Two transforms namely PCT and POT are there in LBT. The lapped transform can be obtain upon the cascading of POT and PCT, LBT can be obtained. In PCT, transformation can be applied for each stage. It is necessary to represent PCT into a polynomial expansion in order to enhance the visual quality by JPEG-XR/HD. POT is not needed always where as PCT must be applied for each block of a macro block. The color conversion is needed to align to the properties of human eyes [19-20].



Fig. 2Proposed PCT System architecture

The key challenges in the design of PCT hardware are the number of multiplexers, adders and the operating speed. Likewise, in the design of photo overlap transform (POT) architecture, block noise edges of the block becomes an important bottleneck that decides the architectural complexity and the hardware cost [21-22]. In the separable method of PCT architecture, PCT can be applied for the decomposition of an image into frequency components shown in figure 2.

3. PCT ARCHITECTURE

For pulse core transform system for high definition photo, the VLSI architecture has been proposed in this paper and is shown in figure 3. PCT based JPEG-XR/HD can save data format when compared to JPEG[23]. Transformation of a time signal into a representation of a small wave having varying frequency on limited duration can be done with the help of discrete wavelet transform(DWT).Using DWT, given signal frequency decomposed into highest frequency and lowest frequency components[24-25].

The given image has been divided into macro blocks. Macro blocks are divided into blocks which are further divided into tiles. Tiles structure is more suitable for an efficient memory buffer size and hardware implementation as shown in figure3. Usually prefilter is used for better image quality and suitable compression ratio considerations at large quantization levels [26-27].



Fig 3. Computational PCT architecture

4. CIRCUIT OF A IMPROVED PARALLEL PROCESSING OF LBT ARCHITECTURE

The traditional LBT architecture increases the delay due to sequential operation of PCT and POT. Sequential processing leads to more delay. This creates longer critical path of the architecture [28-30]. Hence, this longer critical path has been reduced by a parallel processing technique as illustrated in Figure 4.



Fig. 4 Improved parallel processing of LBT architecture

4.1 Encoding Process

When compared to JPEG2000, JPEG-XR/HD proved to be better for digital cinema (DC) compression. In order to obtain. 15 AC coefficients and 1 DC coefficient, a 4x4 Pulse core transform is applied to each block same as DCT in JPEG as shown in figure 4. DC block can be resulted by the collection of all the DC coefficients. JPEG-XR/HD is used to transform the image into blocks and the blocks are transformed into coefficients [7].



Fig. 5 Generation of DC and AC coefficients

It has been shown that the Very large scale integration(VLSI) architecture reduces hardware in the design, the effective longest path and accomplish least power consumption. To compute the operations, the modified systolic array VLSI architecture uses pipelining. Adders and multiplexers are there in the systolic array VLSI architecture. This architecture proved to be an energy and area efficient VLSI architecture for the implementation of PCT [5]. In [3], extra registers are used to achieve pipelining for better performance at the expense of more hardware which is responsible for slow down the compression process. Hence in this paper, less number of registers are used by introducing redundancy to enhance the speed of the JPEG-XR encoder. An effective design of PCT for reducing memory requirements to a great extent are presented in this work [8].

5. DIFFERENT TYPE OF TECHNIQUES USED BY PHOTO CORE TRANSFORM (PCT)

5.1 Lapped Bi-orthogonal transform

The proposed PCT has been implemented to achieve less power consumption using Xilinx 14.7. Different performance metrics such as Power (mW), propagation delay (nS), performance (MHz) etc. are analyzed and recorded. In this proposed work, 16-bit adder and shifter circuits and parallel multiplier circuit were implemented. Thus, the proposed PCT architecture enhances the speed of the design due to the reduction in the area and delay. Thus, the photo core transform was developed to obtain less power and high speed. The simulation and synthesis can be done using VHDL language in Modelsim. The proposed PCT architecture can be implemented using VHDL and the results are showing in figure 6.



Fig. 6 Register transfer logic schematic of PCT

The PCT, Register transfer logic schematic is shown in figure 6. The diagram shows less number of registers required for the development of JPEG-XR image compression system.

b) Technology Schematic of PCT



Fig. 7 Technology Schematic of PCT

The technology schematic of PCT is shown in figure 7. The technology schematic shows that less area can be utilized for the design of JPEG-XR image compression system.

 Table 1. Parameter's comparison of PCT Outputs for existing and proposed solution

Parameter	Existing system[1]	Proposed system
Power(mW)	5.7	4.4
Delay time(ns)	4.702	3.554
Performance(mHz)	50	135

 Table 1 shows the speed, power and delay comparison of proposed system with the existing system.

 Using Xilinx ISE the redesigned PCT architecture has been

implemented. From the area and power consumption point of view there is a better improvement when compared to the existing architectures found from the results. The PCT has been implemented in the FPGA device **Xilinx** Zynq-7000. The device utilization summary is shown in figure 8.

Hardware utilization	Used	Available	% of Utilization
LUTs	125	1214	10.29
Muxs	252	2560	9.84
IOBS	122	520	23.46
Power			
Consumption	290mW		
Delay	28.7ns		

Fig 8. Device utilization summary

The power-related calculations are shown in figure 9.This JPEG-XR design consumes less power when compared to the other image compression techniques. The dynamic power proved to be less when compared to the existing architectures. The static power consumption proved to be very small and it can be neglected.

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Fig 9. XILINX Power Estimator

5.2 Data Reuse Architecture for Lifting PCT

In the data reuse technique shown in Figure 10, filtering operations are computed for a block of row instead of single row performance. Each block of image is applied with PCT row wise filtering operation and the outputs are stored in a vertical manner. Again, PCT operation is computed on the vertical data to complete the LBT operation and it generates DC, AD and AC frequency sub bands. The synthesis results are taken by applying various types of images with different file sizes.



Fig 10. Building blocks of data reuse architecture

 Table 2 furnishes the comparative results of the proposed method with the existing methods for a block size of 4.

 Table2 Comparative results of existing architectures with data raws erabitation

Designs	Bloc k size	Area (u. sqm)	Powe r (mW)	Dela y (ns)	I/O Pin s
(Simonea. F. D. 2007)	4	977829.28	8.92	11.0 6	65
(S. Zhang. 2015)	8	1493335.8 8	12.24	15.5 2	83
Maalouf et.al 2009)	8	1485741.9 6	10.45	16.9 5	82
Data reuse architectur e (proposed)	8	8,75,633.1	7.90	15.4 3	72

 Table 2.Synthesis results of the data reuse architecture for different image sizes

5.3 Using MATLAB

JPEG 2000 is indeed an improvement over the traditional JPEG. Despite the advancements in newer compression standards, JPEG remains widely used, partly due to its long-standing presence and compatibility across various devices and platforms. Absolutely, data compression plays a crucial role in various domains, and one of its primary advantages is the efficient utilization of storage space. JPEG-XR/HD, also known as HD Photo or Windows Media Photo, was indeed a newer image coding standard introduced by the Joint Photographic Experts Group (JPEG) committee. JPEG-XR (or HD Photo) was indeed known for using the Lapped Biorthogonal Transform (LBT) and advanced Huffman coding for image quality than traditional JPEG for the same

amount of data and JPEG-XR/HD supports both lossy and lossless compression modes. Striking a balance between higher compression ratios and better visual quality is essential to meet the requirements of modern applications across various domains.

In this paper, a three-stage pipelining of lossless JPEG-XR encoder has proposed to process the capacity and hardware utilization All the transform operators are implemented as lifting steps using only integer operations. This work shows how lossless and lossy compression of multiple HDR formats can be achieved using JPEG-XR codec with better compression efficiency and less computational complexity due to the arithmetic calculations on integers. The proposed design can be suitable for HDR formats effectively. For future research the high performance hardware implementations of PCT is necessary.

The PCT has been implemented to perform lossless image compression images using MATLAB. The values for different performance metrics like compression Ratio (CR), Peak Signal-Noise-Ratio (PSNR), Mean Square Error (MSE) etc. are analyzed and recorded. Using MATLAB for image processing research is a common and beneficial choice for several reasons. MATLAB, a high-level programming language and environment, is widely adopted in the field of image processing for various inherent characteristics. MATLAB basic data element is an array that doesn't require explicit dimensioning. This aspect of MATLAB significantly simplifies the handling of matrix and vector formulations.

An image is nothing but a matrix or set of matrices which define the pixels value of the image, such a gray scale value in black and white images and Red, Green and Blue or Hue, Saturation and Intensity values in color images. The simulation results using MATLAB for various images are shown in figure 11.









Fig 11. Simulation Results For women image

 Table 3 shows the Image quality parameters comparison of

 PCT Outputs for different Images

IMAGE TYPE	PSNR(dB)	MSE	COMPRESSION RATIO (CR)
GIRL.jpg	11.198	4934.31	2
ROSE.jpg	6.781	13637.81	1
HEART.jpg	14.152	2499.5	2
FLOWER.jpg	8.15	10057.7	0.019
LENA.jpg	7.631	11218.3	1

It is observed that the simulated results are in close agreement with the measured values with respect to PSNR and MSE. It is also observed that the JPEG-XR/HD system is greatly influenced by the photo overlap transform and photo core transform. Since high-performance image compression systems are of great importance in the internet and medical applications, besides medical image systems, the JPEG-XR/HD system is also analyzed, modeled and synthesized for medical image applications. These compression systems are expected to cover large number of images and yet the JPEG-XR/HD system is expected to be efficient, less computationally intensive, economical and highly reliable. The results from the analysis of JPEG-XR give us confidence that the system can be used in contemporary internet systems, satellite imagery systems and for medical applications.

5.4 Development of Systolic Array VLSI Architecture For JPEG-XR System

Lapped bi-orthogonal transform (LBT) based JPEG-XR coding offers improved performance against the other image compression methods like vector quantization, JPEG and JPEG 2000. JPEG-XR/HD algorithm is one of the Lapped biorthogonal transform based still image encoding algorithms, which continuously generates scalable bit stream. It means that a particular encoded bit stream can be used to create images at various bit rates and quality without compromising the compression. The decoder can stop the process of decoding once the target rate or the expected image quality has arrived. JPEG-XR/HD algorithm is developed from Lapped bi-orthogonal transform (LBT). The main advantages of JPEG-XR/HD coding are the integer operations and the distortion scalability. The distortion scalability can be embedded in the progressive transmission. The primary important information is transmitted first during the progressive transmission and then the least important information.

VLSI algorithms and architectures for computation of pulse core transform (PCT) are presented here. In the context of the JPEG-XR/HD standard, the lifting-based architecture is more suitable compared to the convolution-based architecture because of the inherent features of lifting-based implementation of PCT.

The PCT computation module computes the multilevel decomposition of the input image macro blocks. At each step, PCT will produce DC, AD, AC components shown in figure 12. The sub band DC is input back to the PCT modules for the next level of decomposition. The other two sub bands are

input to the subsequent phases of the architecture for entropy encoding.





of JPEG-XR/HD Encoder

Systolic arrays are a type of parallel computing architecture known for their regular and structured design, particularly well-suited for applications involving large-scale computations, such as signal processing and matrix operations. When dealing with large filter lengths, systolic arrays offer several advantages in terms of efficiency and VLSI. The transfer of data play a vital role in determining the efficiency of the VLSI implementation of lifting based PCT.

5.5 Hardware Implementation Using FPGA Device

Software implementation alone does not assure the performance of JPEG-XR/HD image compression system. Hence, real time development can be done through the dedicated hardware. In hardware implementation, architecture plays a vital role which decides the throughput, area and power consumption of the design. Minimized architecture design consumes less hardware. An efficient Architecture reduces the power consumption and area. Power consumption and area are the major requirements for portable devices operated using batteries. The cost of any device can be made cheaper by using small silicon area. Lower power consumption brings more life to the battery.

To validate the performance of the JPEG-XR/HD coder, the comparative device utilization summary evaluated by the Xilinx simulation software and PCT coder are listed in Table 4. The results show that the proposed coder utilizes fewer resources as compared with traditional DWT coder. The less resources utilization in the FPGA device reduces the hardware complexity of the system. It is observed that the proposed method saves 52% of area compared with conventional method and 22 % increased speed of operation at the cost of increased number of memory units.

6. CONCLUSION

In this paper, the PCT was developed to reduce 43.4% memory from external memory. An area efficient photo core transform was designed for the effectiveness of JPEG-XR. The proposed photo core transform was implemented using modified multiplier, shifter and adder for the reduction in power consumption. The recommended design can be suited for HDR formats effectively. For further research an efficient PCT is implemented for better performance with reduced hardware implementations.

Future scope: using cadence 180nm CMOS technology, create a high-precision PCT system for JPEG-XR image compression system with Improved parallel processing of LBT architecture. In further research it is possible to design and implement a JPEG-XT image compression system with the concept of hamming distance.

REFERENCES

- Dufaux, F., Sullivan, G.J., and Ebrahimi, T.(2009). The JPEG XR image coding standard [standards in a nutshell], IEEE Signal Process. Mag. 26, (6), pp. 195–199, 204-204, <u>doi: 10.1109/MSP.2009.934187</u>.
- ISO/IEC 29199-2.(2012) Information technology JPEG XR image coding system--<u>Part 2:Image coding specification</u>.
- Perra, C.(2013).Re-encoding JPEG images for smart phone applications. Proc. IEEE 21st Telecommunications Forum, Belgrade, Yugoslavia, November, pp. 955–958, <u>doi: 10.1109/TELFOR.2013.6716389</u>.
- Maalouf, A., and Larabi, M.C. (2009). Low-complexity enhanced lapped trans-form for image coding in JPEG XR/HD Photo '. 16th IEEE Int. Conf. on Image Processing, Cairo, Egypt, November, pp.5–8, <u>doi:</u> <u>10.1109/ICIP.2009.5413933</u>.
- Tu, C.J., Srinivasan, S., Sullivan, G.J., Regunathan, S., and Malvar, H.S. (2008).Low- complexity hierarchical lapped transform for lossy-tolossless image coding in JPEGXR/HD photo . Proc. SPIE Applications of Digital Image Processing XXXI, San Diego, USA,August, pp. 70730C-1 – 70730C-12, doi: 10.1117/12.797097.
- Tseng, C.-F., and Lai, Y.-T.(2012).Hardware-software co-design architecture for joint photo expert graphic XR encoder', IET Image Process, 6, (9), pp. 1284 –1292, <u>doi: 10.1049/iet-ipr.2011.0491</u>.
- Tinku Acharya,Ping-SingTsai.(2005).JPEG2000 standard for Image Compression: Concepts, Algorithms and VLSI Architectures -Wiley,2005 Edition
- ISO/IEC FDIS 29199-2 | Draft ITU-T Rec. T.832.(2009).Information technology – JPEG XR image coding system – Image coding specification, JPEG document WG 1 N 4918, Feb.
- D. Schonberg, S. Sun, G. J. Sullivan, S. L. Regunathan, Z. Zhou, and S. Srinivasan.(2008). Techniques for enhancing JPEG XR / HD Photo ratedistortion performance for particular fidelity metrics, <u>SPIE Appl. of Dig.</u> <u>Image Proc. XXXI, vol. 7073, paper 7073-41</u>, Aug.
- G. J. Sullivan, S. Sun, R. Rossi, S. L. Regunathan, and Zhi Zhou.(2008).Image Format Support and Color Handling Aspects for JPEG XR, JPEG contribution WG 1 N 4680, July.
- H. S. Malvar and D. H. Staelin.(1989). The LOT: transform coding without blocking effects," IEEE Trans. <u>on Acoustics, Speech, and Signal Processing, vol. 37, pp. 553-559</u>, April.
- H. S. Malvar.(1998).Biorthogonal and nonuniform lapped transforms for transform coding with reduced blocking and ringing artifacts, IEEE Trans. Signal Processing, pp. 1043-1053, April.
- 13. ITU-T SG 16 Q.6 and ISO/IEC JTC 1/SC 29 WG 1.(2008).Study Text for JPEG XR FCD (ISO/IEC 29199-2)", Document N4659, June.
- D.D.Giusto, T.Onali.(2007).Data Compression for Digital Photography: Performance comparison between proprietary solutions and standards, <u>IEEE Conf. Consu. Elec.</u>, pp. 1-2.
- S. Srinivasan, Z. Zhou, G. J. Sullivan, R. Rossi, S. Regunathan, C. Tu, and A. Roy.(2008).Coding of high dynamic range images in JPEG XR /

HD Photo, Applications of Digital Image Processing XXXI, Proceedings of SPIE, vol. 6696, Aug.

- C.-H. Pan, C.-Y. Chien, W.-M. Chao, S.-C. Huang, and L.-G. Chen.(2008).Architecture design of full HD JPEG XR encoder for digital photography applications, <u>IEEE Trans. Consu. Elec.</u>, Vol. 54, <u>Issue 3</u>, pp. 963-971, Aug.
- D. Schonberg, S. Sun, G. J. Sullivan, S. Regunathan, Z. Zhou, and S. Srinivasan. (2008). Techniques for enhancing JPEG XR / HD Photo ratedistortion performance for particular fidelity metrics, Applications of Digital Image Processing XXXI, <u>Proceedings of SPIE</u>, vol. 6696, Aug.
- S. Srinivasan, C. Tu, S. L. Regunathan, and G. J. Sullivan.(2007).HD Photo: A new image coding technology for digital photography, Applications of Digital Image Processing XXX, <u>Proceedings of SPIE</u>, vol. 6696, San Diego, CA USA, August.
- Prasanna kumar Godi,Krishna T Battula and Pushpa Kotipalli.(2020). Radix-4 feedback design using four parallel adders with efficient Reordering module for fast fourier transform",Journal of advanced research in dynamic and control systems ,12(3):593-598,January.
- 20. S.Siva Parvathi Lakshmi Durga , Satyanarayana Murty P and K. Srinivas.(2008).Dual Digital Signature Using Stationary Wavelet Transform singular Value Decomposition", <u>Global Journal Of</u> <u>Engineering Science And Researches</u>, ISSN 2348 – 8034,pp:522-531,June.
- Y. Tang, T. Xiang, Y. Yang and Z. Shu.(2020).JPEG-XR-GCP: Promoting JPEG-XR Compression by Gradient-Based Coefficient Prediction,12th International Conference on Advanced Computational Intelligence (ICACI), pp. 51-58, August.
- Abhishek baba, Rakesh Biswas.(2021).Pipeline Architecture of Forward and Inverse Photo Core Transform for JPEG XR Image Compression, <u>International Conference on Intelligent Technologies (CONIT)</u>, June.
- 23. Abhishek Baba, Rakesh Biswas.(2021).Multiplier-less Lifting-based Photo Core Transform for JPEG-XR Ultrasound Image Compression, 2nd International Conference for Emerging Technology (INCET),May.
- Koichi Hattori; Hiroshi Tsutsui; Hiroyuki Ochi; Yukihiro Nakamura.(2009). A high-throughput pipelined architecture for JPEG XR encoding, IEEE/ACM/IFIP 7th Workshop on Embedded Systems for Real-Time Multimedia, DOI: <u>10.1109/ESTIMedia15925.2009</u>.
- Taingliv Min; Supavadee Aramvith. (2022). Performance Analysis of JPEG XR with Deep Learning-Based Image Super-Resolution, Asia-Pacific Signal and Information Processing Association Annual Summit (APSIPAASC), DOI: <u>10.23919/APSIPAASC55919.2022.9980019</u>.
- Antonio Lopes Filho, Roberto Damore.(2021). FPGA implementation of the JPEG XR for onboard earth-observation applications, Journal of Real-Time Image Processing 18(6):1-12, DOI: <u>10.1007/s11554-021-</u> <u>01078-y</u>.
- Abhishek Baba,Rakesh Biswas.(2021).Pipeline Architecture of Forward and Inverse Photo Core Transform for JPEG XR Image Compression, International Conference on Intelligent Technologies (CONIT),DOI: <u>10.1109/CONIT51480.2021.9498482</u>
- Antonio Lopes Filho, Roberto d'Amore.(2021). FPGA implementation of the JPEG XR for onboard earth-observation applications, Journal of Real-Time Image ProcessingVolume 18,Issue 6,Dec,pp 2037–2048, <u>https://doi.org/10.1007/s11554-021-01078-y</u>.
- Yongjun Zhu, Wenbo Liu, 1Qian Shen, Yin Wu and Han Bao. (2020). JPEG Lifting Algorithm Based on Adaptive Block Compressed Sensing, Array Signal Processing with Imperfect Scenarios, Volume 1, Article id 2873830, https://doi.org/10.1155/2020/2873830.
- Roman Starosolski.(2020).Reversible Denoising and Lifting Based Color Component Transformation for Lossless Image Compression, Multimedia Tools and Applications,79(17-18):11269-11294, <u>https://doi.org/10.1007/s11042-019-08371-w</u>.

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