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Design and analysis of a low noise amplifier at 5GHz for IoT applications

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ABSTRACT

This paper presents a low-power Low Noise Amplifier (LNA) for the 5-GHz frequency band. The operating voltage of this Low Noise Amplifier is 1 V. Capacitive Coupling is used for gain boosting. By using these techniques forward-body-bias and Current-reuse DC power dissipation is reduced. The simulation result shows the Noise Figure (NF) of 3 dB and 19 dB of gain at 5-GHz with 1 V operating voltage & power dissipation is 0.62 mW. This LNA is implemented using a 180 nm TSMC library. Employing a modified current-reused architecture, the low-noise amplifier (LNA) can operate at a very low supply voltage with microwatt power consumption while maintaining reasonable circuit performance at 5 GHz.

KEYWORDS

Capacitive Coupling, Forward body bias technique, Forward gain, Low noise amplifier, Noise figure,

1. INTRODUCTION

The revolution of IoT (Internet of Things) brings exclusive changes in the field of wireless communication. Due to huge advancements in wireless communication, day-by-day snags are eliminated to make it comparable with the ideal LNA [1]. The use of CMOS technologies for the implementation of front-end electronics in a GPS is therefore attractive because of the promise of integrating the whole system on a single chip [3]. In wireless communication systems, the LNA plays an important role as the first stage amplification in the receiver such as signal amplification and noise immunity affecting the post-amplifier. When the signal couples from the antenna into an LNA circuit, the signal is amplified and transmitted to a mixer system including the reduction of the noise coming from outside or circuit inside. With the assistance of the ADS simulation software and the adoption of the TSMC 0.18um CMOS process, a promising LNA circuit operated at 5 GHz was implemented. This circuit not only demonstrated a high gain performance but represented excellent isolation. Furthermore, the noise resource is the other factor dominating the performance of a LNA. Basically, the noise coming from the circuit devices, such as shot noise, thermal noise, and flicker noise, must be suppressed well [6]. The overall performance of the receiver system depends on the LNA noise figure and gain. The design of LNA faces several challenges such as linearity, low noise figure (NF), impedance matching, sufficient gain, and low power consumption because it should achieve high gain to suppress the noise. We try to design LNA such that it should provide a minimum noise figure while providing sufficient linearity with gain, IIP3 and a stable 50 Ω input impedance [2]. For minimizing the power dissipation (pdc), some of the techniques are used name as follows reused [1] and forward-body-bias [2]. Enhancing the gain performance and minimize the NF of the Low Noise Amplifier we use Amplifier we use here a topology named as Capacitive Coupling [1]. Good input matching is critical when a preselect filter precedes the LNA. The application of LNA is to amplification before the mixer [2].

The rest of this research paper is described as follows: Section II describes the Capacitive Coupling technique, Designing and implementation of linear ultra-low-power LNA in Section III, and Simulated Results and conclusion are carried out in Sections IV and V respectively [1].

1.1 Capacitive Coupling

Capacitive coupling is the transfer of alternating electrical signals or energy from one segment of a circuit to the other using a capacitor. The coupling provides a medium for the AC signals while blocking the DC energy. As shown in the circuit diagram we are using the capacitive coupling in the input stage of LNA i.e. in the input MOSFET which is CG configured due to this Noise Figure is minimized sponge with the increment in gain. As shown in the circuit diagram of LNA there is two inductor L_6 and L_7 which worked earlier as a mutual inductor that takes a larger place when we design IC of this but to use this capacitive coupling (C_6) by ending the mutual inductance we can see it gives better result than that and it also decreases the size of our IC. Capacitive Coupling (C_6) is shown below in the given circuit [1].

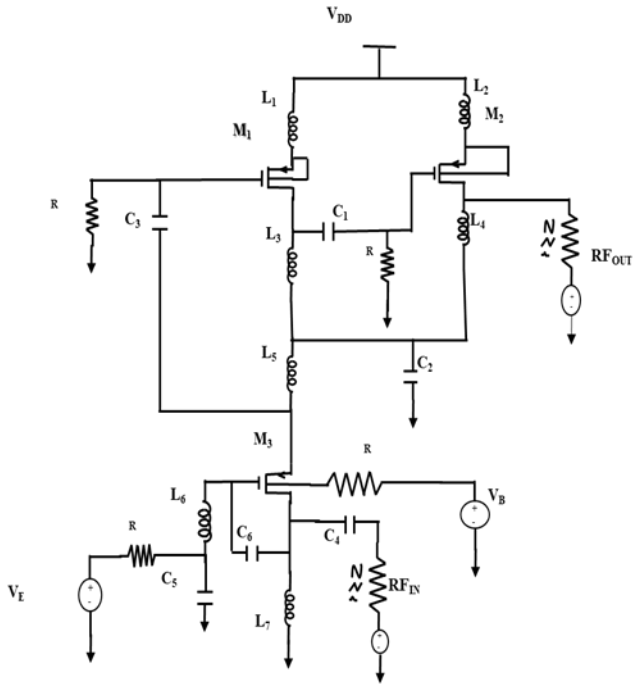

Fig.1 Capacitive coupling

1.2 Current reuse method

The current reuse topology may provide the best combination of high-power gain, low noise figure, and low power consumption, making it a feasible option for use in UWB LNA designs. In an amplifier employing current-reuse techniques, the input RF signal is amplified by two cascaded common-source amplifier stages to provide high gain. The basic issue with using a CMOS transistor for LNA is its inherently low transconductance and hence low gain. However, if the current reuse method is used, transconductance would be increased. The key point is that given the same bias current the effective transconductance is gm1×gm2, while it is simply gm in other cases. A single source results in less power dissipation. The current reuse model can be considered as a two-stage cascade.

amplifier, in which the first stage is the CS amplifier, and the second stage is the cascade amplifier with an additional buffer stage at the output end. The current reuse technique is well known for its use in LNAs and for its capability of achieving high performance with power consumption that is less than conventional two-stage common-source amplifiers. Fig. 4 .1 shows a current reused LNA. The proposed LNA is being described. Since transistors M_1 and M_3 are connected in a current reuse structure, M_1 and M_3 share the same bias current

from the supply voltage. The current reuse LNA. Supports high gain and low power consumption. The capacitor C6 is used to reduce gate-induced noise. The AC signal is amplified by the main transistor M_3 and is coupled to the gate of common source stage M_3 by the capacitor C_3. The two-stage configuration increases the gain. The LNA is biased in a strong inversion region. C_5, L_6, and L_7 R are the input-matching network components. L_1 and C_1 are the output-matching network components. Inductor L_5 is used to provide high impedance between two stages [9]. Fig. 2 Current reuse in Schematic of Proposed LNA

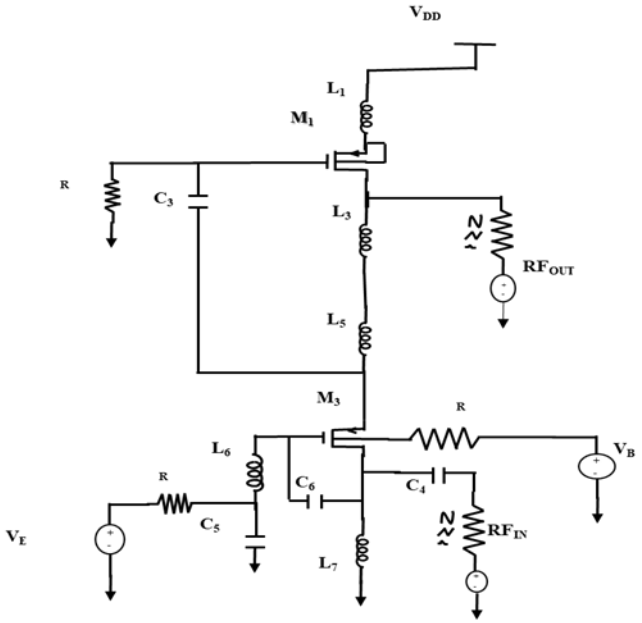

Fig. 2 Current reuse technique used in proposed LNA

2. CIRCUIT DESCRIPTION

For LNA design, the input impedance and noise matching is a design trade-off. In the first stage, we use transformer-coupled common-gate (CG) with forward-body bias and capacitive coupling. In that work, we can achieve impedance and noise matching simultaneously except for the optimization of the matching network, the Gm-boosted common-gate device is the main reason that gain and noise become closer. From its equivalent small-signal model, the resulting noise factor and transconductance is calculated to be

$$F = 1 + \frac{\gamma}{\alpha(1+a)} \qquad (1)$$

$$G = (1+nk)\, g_m \qquad (2)$$

The gain-boosted factor, A=nk, is determined by the turn ratio and the coupling factor of the transformer. The transformer-coupled increases the effective transconductance by (1+A) times and decreases the noise factor by the same factor, where -A is the gain from source to gate. It's attractive to adopt a current-reused topology in low-power LNA because the bias current is shared between multiple gain stages. We combine current-reused topology, transformer-based gain-boosting feedback technique, and forward-body bias technique to achieve the best gain performance in the lowest DC power consumption. For the operation of LNA at low supply voltage and low power dissipation with sufficient gain we add a technique in the gain-boosted common-gate stage named as forward body bias. The threshold voltage of MOSFET is as follows [6].

$$V_{th} = v_{th0} + \gamma(\sqrt{(2_{\varphi}f - v_{bs})}\sqrt{(2_{\varphi}f - v_{bs}} - \sqrt{(2_{\varphi}\_f)} \qquad (3)$$

3. MEASUREMENT RESULTS

This low-power LNA is based on 5-GHz band applications. This LNA has been implemented in 180nm CMOS process using the software Advanced Design System (ADS). In this Low Noise Amplifier drain, gate bias and body bias voltages are 1 V, 0.5 V and 0.29 V respectively. It draws 777 µA current from the supply voltage 1 V. In this LNA the power dissipation (Pdc) is 0.48 mW. The simulated results are shown in Figure 3, 4, and 5. As we can see S- parameters of this LNA, in figure 3 the power gain (S_{21}) is 19.228 dB and input return loss (S_{11}) is 14.3137 dB is shown in fig. 4. NF is 3 dB as shown in fig. 5. Here IIP3 which is also called as third order-intercept is 0.541 dBm. In this LNA 3 dB Bandwidth is 0.25 GHz and - 8.63 dBm is the output of 1-dB compression point (P1 dB).

Table 1 Parameters of proposed LNA

Devices	Values
M_1	84 µm/0.18 µm
M_2	75 µm/0.18 µm
M_3	74 µm/0.18 µm
R_1	10 kΩ
R_2	7 kΩ
R_3	8.5 KΩ
R_4	10 KΩ
L_1/L_2	250 pF
L_3	3 nH
L_4	900 pF
L_5	4 nH
L_6	6 nH
L_7	6.4 nH
C_1/C_3	2 pF
C_2	18 pF
C_4	6 pF
C_5	13 pF
C_6	2 pF

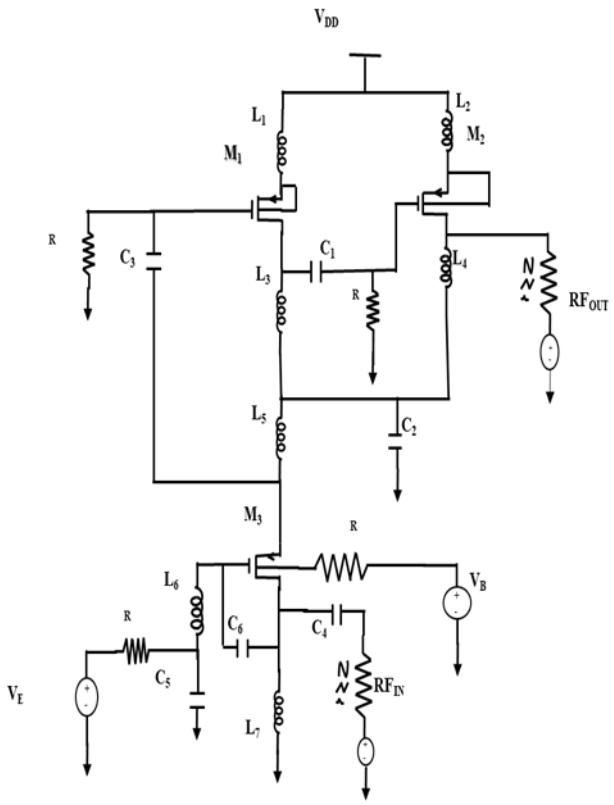

Fig. 3 Schematic of Proposed LNA

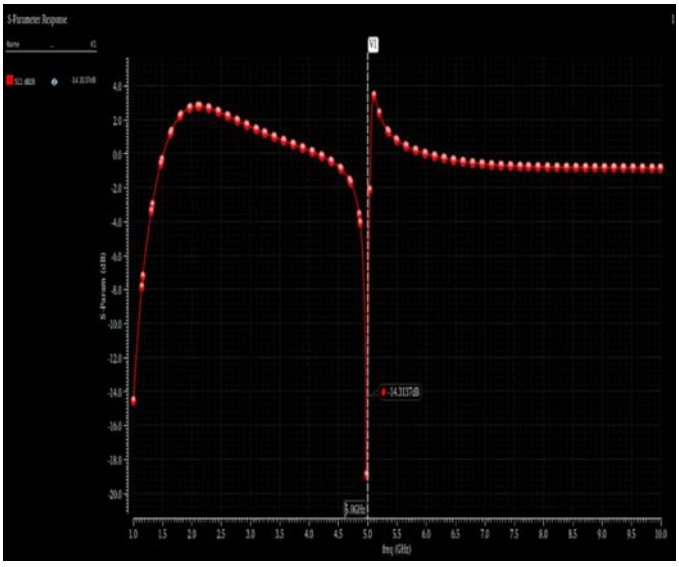

Fig. 4 Plot of input return loss(S_{11}): - 14.3137dB

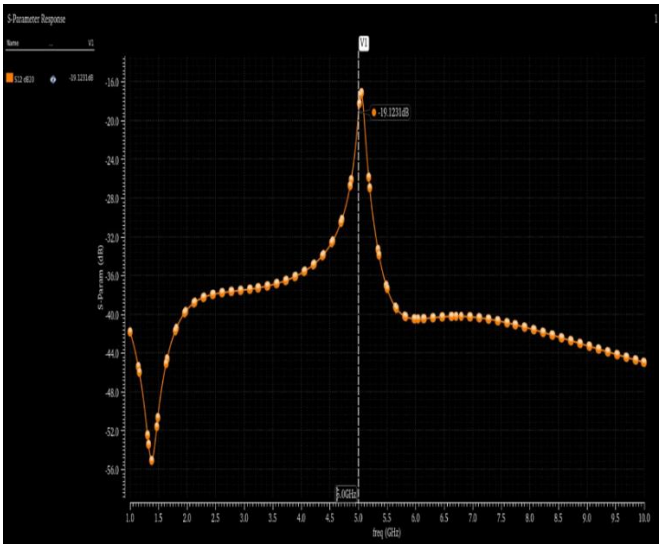

Fig.5 Plot of reverse isolation (S_{12}): - 19.1231 dB

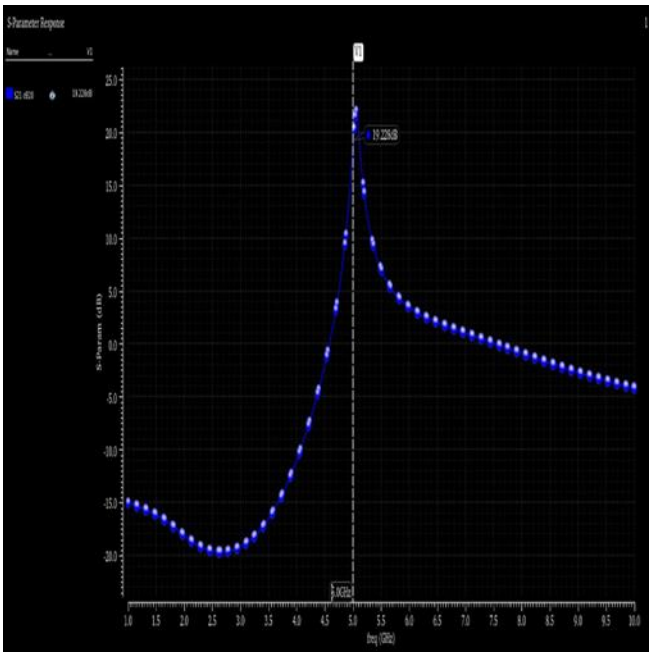

Fig.6 Plot of forward voltage gain (S_{21}): 19.228

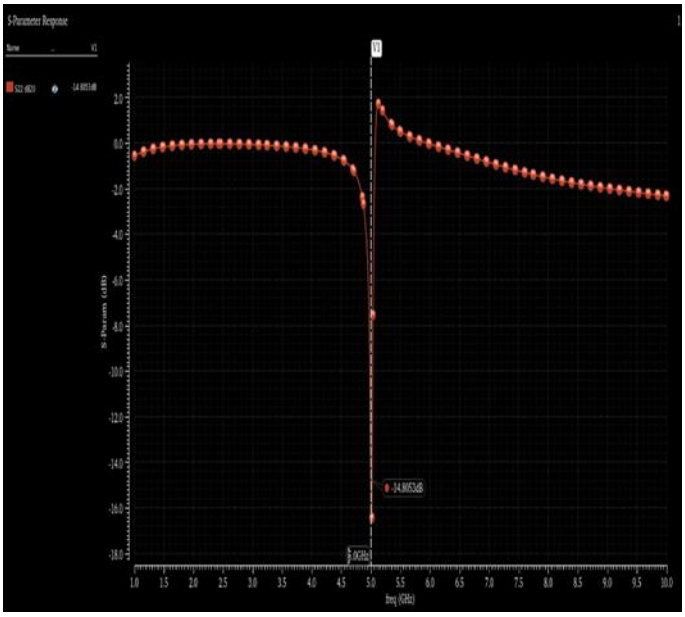

Fig.7 Plot of output return loss (S_{22}): - 14.8053

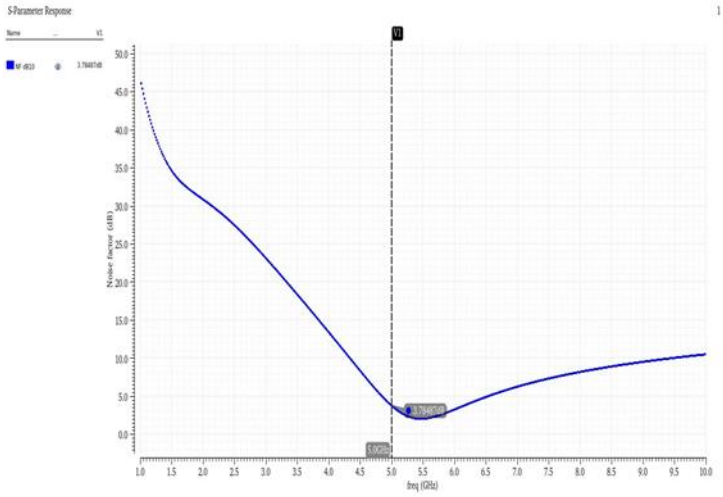

Fig.8 Plot of noise figure 3.78487dB

4. CONCLUSION

In this research paper, an ultra-low power Low Noise Amplifier is presented at the 5-GHz band by using CMOS 0.18µm process. In the first step by combining current reuse, transformer coupled feedback gain boosting, and forward body bias this Ultra-low power Low Noise Amplifier is optimized at 5-GHz frequency and gives NF and power gain of 8.784 dB and 14.228 simultaneously. But after then using the Capacitor Coupling technique this LNA gives the best result as 3. 7848 dB of NF and 19.228 dB power gain at an operating voltage of 0.63 V and 0.48 mW as DC power dissipation. Finally, the proposed ultra-low-power LNA has its best results as noise, gain performance, and low DC power dissipation, showing a good environment in applications in ultra-low-power wireless systems.

Table 2. Performance comparison of previously reported

CMOS LNAs

Reference Work	[5]	[6]	[7]	[8]	This
Technology(nm)	180	180	180	180	180
Operating voltage	0.63 V	0.6V	1.2 V	1.8 V	1V
pdc	0.387	0.336	1.66	3.42	0.62
frequency	5.0	4.8	3.5	5.8	5.0
Gain	14.7	10	12.5	9.4	19.228
Noise figure	4.3	4.8	3.6	2.5	3.7

REFERENCES

1. Walling J. S., Shekhar S. and. Allsto D. J (2007). A gm Boosted Current Reuse LNA in 0.18µm CMOS: IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, HI, pp,613-616. https://doi.org/10.1109/RFIC.2007.380958
2. Chang C. P., Chen J. H. and Wang Y. H. (2009). A Fully Integrated 5 GHz Low Voltage LNA Using Forward Body Bias Technology: IEEE Microwave and Wireless Components Letters, vol. 19, no. 3, pp. 176- 178.
3. Zhuo, Wei & Embabi, S. & Pineda de Gyvez, José & Sanchez-Sinencio, E. (2000). Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design: Electronics Letters - ELECTRON LETT. 77 - 80. https://doi.org/10.1109/ESSCIR.2000.186458 .
4. Cho, T., Dukatz, E., Mack, M., Macnally, D., Marringa, M., Mehta, S., Nilson, C., Plouvier, L., & Rabii, S. (1999). A single-chip CMOS direct-conversion transceiver for 900 MHz spread-spectrum digital cordless phones: IEEE International Solid-State Circuits Conference. ISSCC. First Edition (Cat. No.99CH36278). https://doi.org/10.1109/isscc.1999.759205
5. Alsuraisry, H., Hsiao, S., Lin, Y., Li, P., Tsai, J., & Huang, T. (2017). A review of microwatt low-noise amplifier for microwave and millimeter-wave IoT applications: IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), 71-73.
6. Hsieh C., Wu M., Cheng J., Tsai J. and Huang T. (2013). A 0.6- V 336-Mw 5-GHz LNA using A low-voltage and gain-enhancement architecture: IEEE MTT-S Int. Microwave Symp. Digest (MTT), pp. 1-3.
7. Wei M. D., Chang S. F., Chang C. W., Han C. H. and Negra R., (2011). A CMOS fully differential current-reuse LNA with gm-boosting technique: Microwave Integrated Circuits Conference (EuMIC), 2011European, Manchester, pp. 378-381.
8. Li X., Shekhar S. and Allstot D. J. (2005). Gm-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18 µm CMOS: IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2609–2619.
9. Lai M. T. and Tsao H. W. (2013). Ultra-Low-Power Cascaded CMOS LNA With Positive Feedback and Bias Optimization: IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 5, pp. 1934-1945.
10. Razavi B., Design of Analog CMOS Integrated Circuit:2nd ed. McGraw-Hill.
11 Razavi. B. (1998). Basic concepts of RF Design: RF Microelectronics University of California, Prentice Hall.
12. Wang M. et al. (2017). A CMOS dual-feedback reconfigurable Low Noise Amplifier with improved stability and Reduced noise: IEICE Lett. https://doi.org/10.1587/elex.14.20170985
13. Huang Y. -W. et al. (2022). A Low Power, Wideband Low-Noise Amplifier with Current-Reused Techniques in 0.18-µm CMOS for 5G Wireless Systems: Asia-Pacific Microwave Conference (APMC), Yokohama, Japan, pp.7-9. doi: https://doi.org/10.23919/APMC55665.2022.9999969
14. Chang F. and Lin Y. -S. (2021). 3–9-GHz CMOS LNA Using Body Floating and Self-Bias Technique for Sub-6-GHz 5G Communications: IEEE Microwave and Wireless Components Letters, vol. 31, no. 6, pp. 608-611. doi: https://doi.org/10.1109/LMWC.2021.3075279
15. B. Park and K. Kwon (2021). 2.4-GHz Bluetooth Low Energy Receiver Employing New Quadrature Low-Noise Amplifier for Low-Power Low-Voltage IoT Applications: IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 3, pp. 1887-1895. doi: https://doi.org/10.1109/TMTT.2020.3041010
16. J. Liu, (2021). Analysis of Low-Noise Amplifier (2021) 6th International Conference on Intelligent Computing and Signal Processing (ICSP), Xi'an, China, pp. 1427-1432.doi:https://doi.org/10.1109/ICSP51882.2021.9408677
17. Li et al. (2023). Analysis and Design of a 2-40.5 GHz Low Noise Amplifier With Multiple Bandwidth Expansion Techniques: IEEE Access, vol. 11, pp. 13501-13509.doi: https://doi.org/10.1109/ACCESS.2023.3243090
18. Jahnavi D., Kavya G. & Banu A.J. (2022). Design and Analysis of 2.4 GHz Low-Noise, High-Gain 0.18 µm CMOS Cascode Low-Noise Amplifier for IRNSS Applications: IETE Journal of Research, 68:6, 3960-3970.

DOI: https://doi.org/10.1080/03772063.2020.1782783

19. Nordic TM, Gounella RH, Luppe M, Junior JNS, Fon off ET, Colombari E, Romero MA, Carmo JPPd (2022).Low-Noise Amplifier for Deep-Brain Stimulation (DBS). Electronics.11(6):939.doi: https://doi.org/10.3390/electronics11060939

20. Jeemon B. K., Veeravalli S. K., Shambavi K. and Z. C. Alex (2013). Design of a high gain low noise amplifier for wireless applications: IEEE Conference on Information & Communication Technologies, Thuckalay, India, pp. 1171-1174.doi: https://doi.org/10.1109/CICT.2013.6558277

21. Zhang J., Zhang H., Sun Q. and Zhang R. (2018). A Low-Noise, Low-Power Amplifier With Current-Reused OTA for ECG Recordings: IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 3, pp. 700-708.doi: https://doi.org/10.1109/TBCAS.2018.2819207

22. Shin W., Callender S., Pellerano S. and Hull C. (2018).A Compact 75 GHz LNA with 20 dB Gain and 4 dB Noise Figure in 22nm FinFET CMOS Technology: IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, pp. 284-287.doi: https://doi.org/10.1109/RFIC.2018.8429036

23. Chen H., Zhu H., Wu L., Xue Q. and Che W. (2022).A 7.2–27.3 GHz CMOS LNA With 3.51 ±0.21 dB Noise Figure Using Multistage Noise Matching Technique: IEEE Transactions on Microwave Theory and Techniques,vol.70,no.1, pp.74-84.doi: https://doi.org/10.1109/TMTT.2021.3121074

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