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Design of common source amplifier with resistive load and diode load with gain comparison

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ABSTRACT
This paper investigates the performance disparity between resistive and diode loads in a Common Source Amplifier (CSA) designed via Cadence Virtuoso software utilizing UMC 90nm technology. The aim was to compare the gain characteristics of the CSA employing these two distinct loads under identical design specifications and operating conditions at a frequency of 100MHz with a 1.8V power supply. The designed CSA circuit incorporated both resistive and diode loads, intending to evaluate their respective gains. Surprisingly, the resistive load exhibited a higher gain of 19.11dB, whereas the diode load demonstrated a lower gain of 15.7dB, despite adhering to the same design methodology and specifications. The discrepancy in gains between the two load types warrants further investigation into the underlying reasons behind this observation. This study serves to highlight the nuanced impact of load selection on the gain performance of a Common Source Amplifier, providing valuable insights into load-dependent variations and their implications for amplifier design and performance optimization.

KEYWORDS
Common source amplifier, Resistive load, Diode load, cadence virtuoso, gain

1. INTRODUCTION

Amplifiers serve as pivotal components in modern electronic systems, playing a fundamental role in signal processing and amplification across various applications. Among the numerous amplifier configurations, the common source amplifier stands out for its simplicity and versatility in amplifying analog signals. One of the critical aspects influencing the performance of such an amplifier is the load connected to its output stage.

This journal article delves into the design and comparative analysis of common source amplifiers employing two distinct load types: resistive load and diode load. The choice of the load significantly impacts the amplifier's gain, bandwidth, linearity, and overall performance. By investigating these two load configurations, this study aims to elucidate the trade-offs and advantages associated with each design.

The resistive load configuration, commonly utilized in traditional amplifier designs, offers straightforward implementation and stability. However, it often presents limitations in terms of gain and efficiency, particularly in high-frequency applications due to its inherent capacitance and limited swing at the output.

On the other hand, the diode load configuration introduces a different approach by employing semiconductor diodes as the load elements. Diode-loaded amplifiers offer potential benefits such as higher gain, improved linearity, and better efficiency compared to resistive loads. The diode load's nonlinear characteristics can influence the amplifier's behavior, posing challenges in biasing and design

In this article, we present a comprehensive comparative analysis of these two configurations by exploring their design methodologies, small-signal models, biasing techniques, frequency responses, and gain performances. Through simulations and experimental validations, we aim to provide a thorough understanding of the advantages, limitations, and trade-offs inherent in each design.

The investigation's findings will contribute to the deeper comprehension of common source amplifiers with resistive and diode loads, aiding engineers and researchers in selecting the most suitable design based on specific application requirements. Ultimately, this comparative study aims to enhance the understanding of load effects on amplifier performance and guide the development of optimized amplifier designs for diverse applications

The paper is organized as section II has the description of the design of a CS amplifier with resistive load, and section III includes a description of the design of a CS amplifier with diode load. The result and discussion are summarized in section IV. Finally, section V is the conclusion of the proposed LNA.

2. DESIGN OF CS AMPLIFIER WITH RESISTIVE LOAD

The schematic diagram of the Common Source Amplifier with resistive load is shown in Figure 2. The two NMOS transistors used here are in current mirror mode. The aspect ratios of the NMOS are equal for a good gain. The design specifications are exhibited in Table1.

Table. 1 Design specifications of Common Source Amplifier with resistive load.

Specification name	Value
V_{dd}	1.8V
A_v	20dB
f_{3dB}	100MHz
C_L	5pF
Technology used	90nm

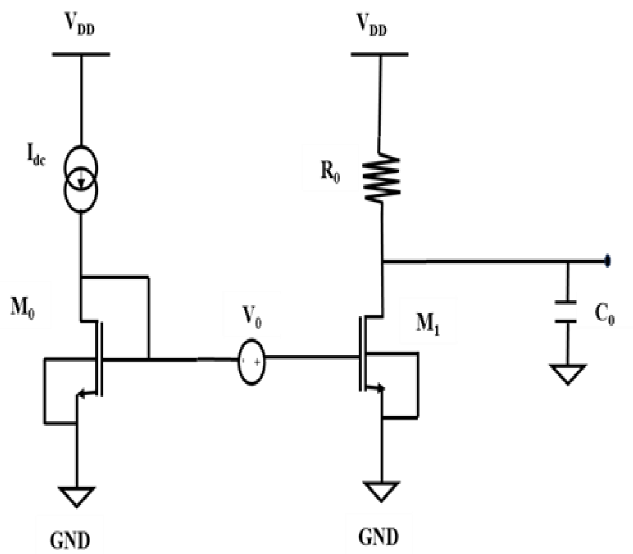

Fig. 1 Schematic diagram of Common Source Amplifier with resistive load

Design parameters are obtained with the following equations

$$f_{3dB} = \frac{1}{2\pi R_L C_L} \quad (1)$$

(R_L is obtained (318Ω)).

$$A_V = g_m . R_L \quad (2)$$

(g_m obtained =31mA/V)

$$Id = \frac{1}{2}\mu nCoxW/l(vgs - vth)vov \quad (3)$$

(obtained I_d=3.1m)

$$g_m = \sqrt{2Id\mu nCoxW/l} \quad (4)$$

3. DESIGN OF CS AMPLIFIER WITH MOS DIODE LOAD

The schematic diagram of the Common Source Amplifier with diode Load is shown in Figure 2.

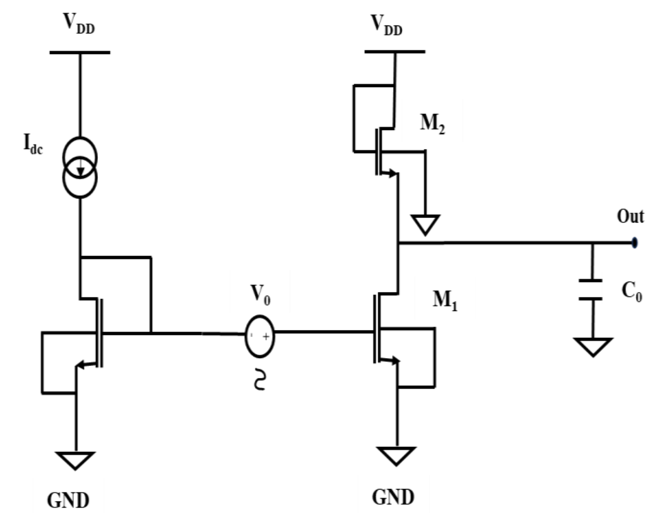

Fig. 2 Schematic diagram of Common Source Amplifier with active diodeload

The two NMOS transistors used here are in current mirror mode [11-16]. The aspect ratios of both the nmos are equal for a good gain. The aspect ratio of the diode load which is also a nmos has the least aspect ratio just enough to push the amplifier into the saturation region [17-20].

The CS amplifier is designed using UMC 90nm technology in cadence virtuoso software for a gain of 20dB at a frequency of 100MHz, the supply voltage is 1.8V and the load capacitance is 5pF.

Design parameters are obtained with the following equations

$$f_{3dB} = \frac{1}{2\pi R_L C_L} \quad (5)$$

(R_L is obtained (318Ω)).

$$A_V = g_m . R_L \quad (6)$$

(g_m obtained =31mA/V)

$$Id = \frac{1}{2}\mu nCoxW/l(vgs - vth)vov \quad (7)$$

(obtained I_d=3.1m)

$$g_m = \sqrt{2Id\mu nCoxW/l} \quad (8)$$

4. SIMULATION RESULTS

The common-source amplifier is a basic unit in many typical analog circuitry cells such as the level converter and output stage. The common-source amplifiers with the Resistive load and diode-connected active-load structures are used to verify the impact of MOSFET gate-oxide reliability on CMOS analog amplifiers [2].

Figures 3-8 show the results (transient analyses, gain in magnitude, and dB) of the CS amplifier of both resistive and diode loads. In Figure 9 it is seen the comparison of gain for both designs is and it can be said that the gain of resistive load is greater compared to diode load. Table 2 shows the comparison of different common source amplifiers.

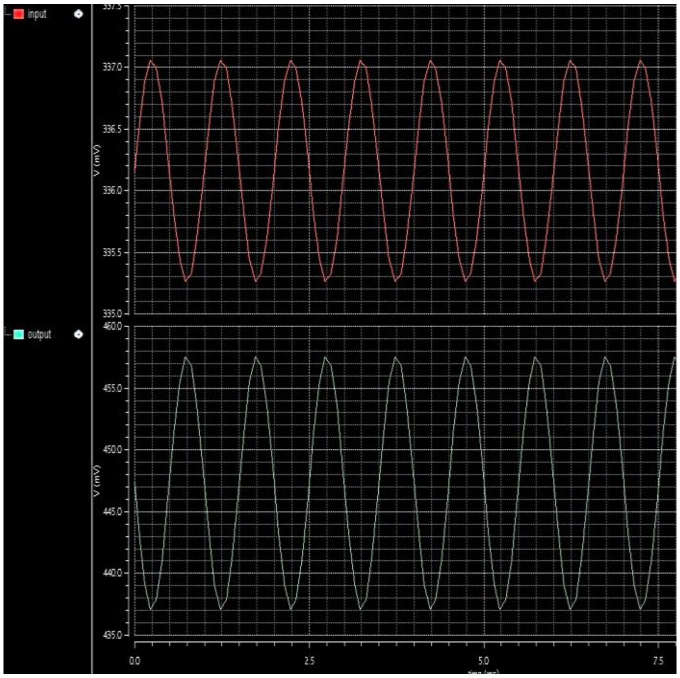

Fig. 3 Transient analyses with V_{in} =1mV

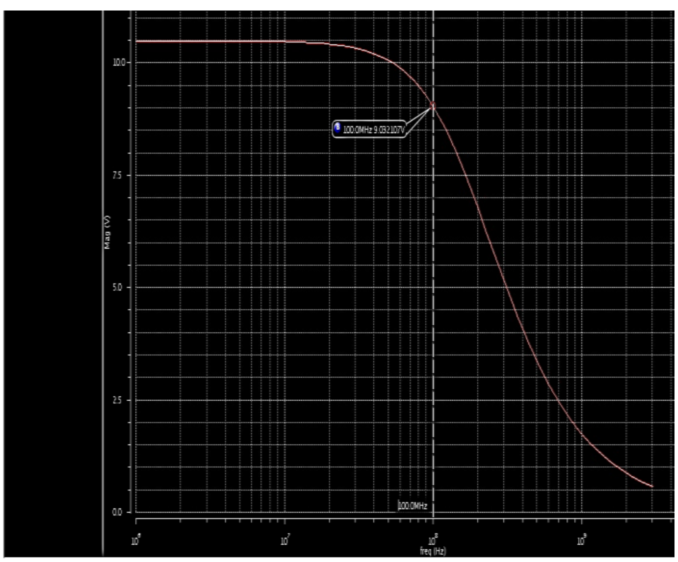

Fig. 4 Plot of gain (|Av|=9.02)

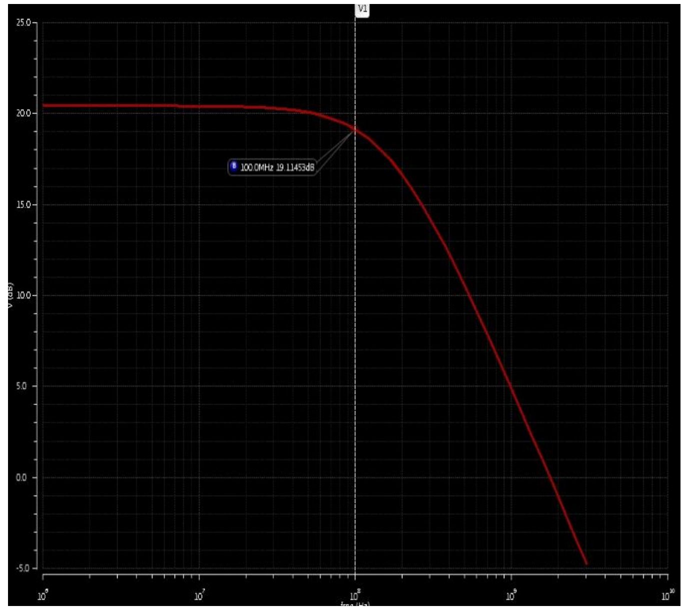

Fig. 5 Plot of gain (|Av|=19.11dB)

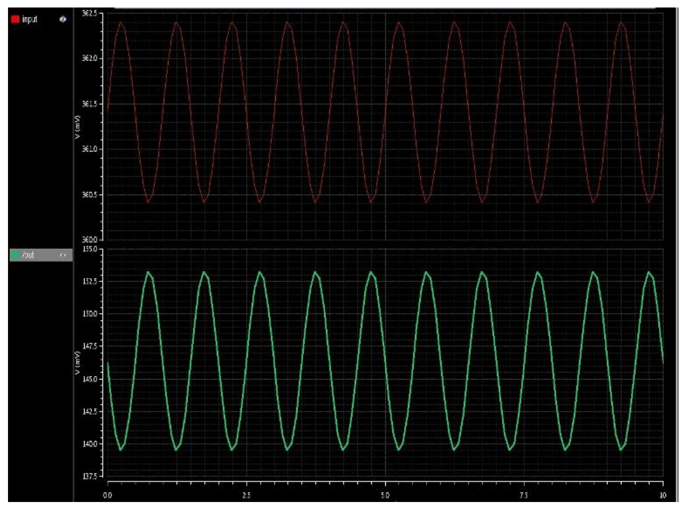

Fig. 6 Transient analyses with Vin =1mV

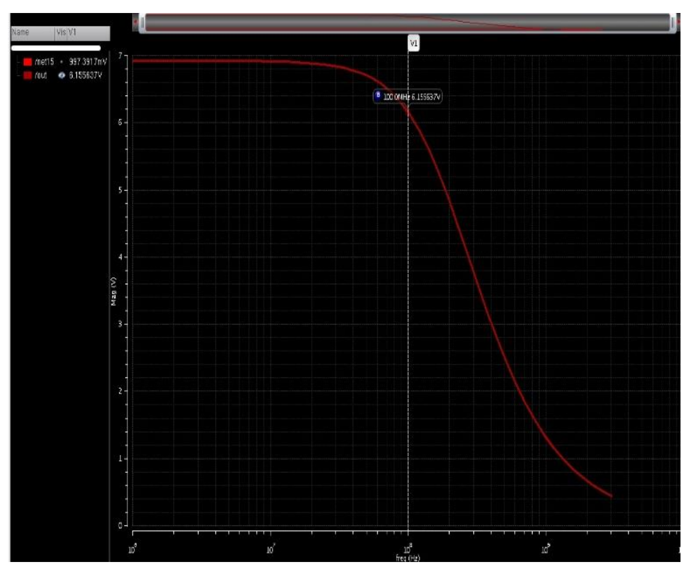

Fig. 7 Plot of gain (|Av|=6.15)

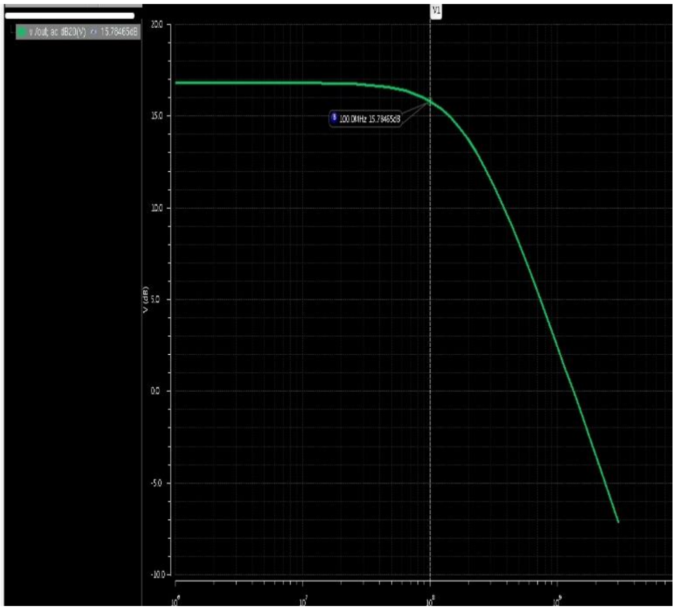

Fig. 8 Plot of gain (|Av|=15.7dB)

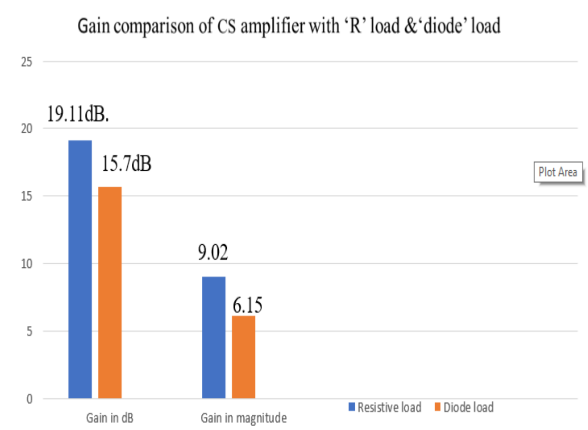

Fig. 9 Gain comparison of CS amplifier with 'R' load and active diode load

5. CONCLUSION

In conclusion, this study extensively explored and compared the performance of a Common Source Amplifier (CSA) utilizing resistive and diode loads in the Cadence Virtuoso software with UMC 90nm technology. Despite the identical design parameters and operational settings at a frequency of 100MHz with a 1.8V power supply, a notable divergence in gain performance was observed between the two load types.

The resistive load configuration exhibited a significantly higher gain of 19.11dB, surpassing the gain achieved with the diode load, which measured 15.7 dB. This unexpected difference in gain performance highlights the intricate influence of load selection on the overall amplifier characteristics.

While the resistive load demonstrated superior gain, the diode load presented a lower gain, indicating potential differences in impedance matching, parasitic effects, or non-linear behavior affecting the amplifier's performance. Further investigations into the underlying factors contributing to this discrepancy are necessary to elucidate the specific mechanisms responsible for the observed variation.

This research underscores the importance of load choice in amplifier design, showcasing how seemingly minor load variations can significantly impact gain characteristics. Understanding and optimizing load-dependent effects are crucial for enhancing amplifier performance and efficiency in various applications.

Overall, this comparative analysis of resistive and diode loads in a Common Source Amplifier provides valuable insights into load-related variations, paving the way for more nuanced amplifier designs and fostering a deeper understanding of load-dependent effects for future electronic circuit implementations.

REFERENCES

1. C S, Sajin & Hameed, Tad. (2020). Review of CMOS Amplifiers for High-Frequency Applications. International Journal of Engineering and Advanced Technology. 10. 175-180. 10.35940/ijeat.B2101.1210220.
2. J. -S. Chen and M. -D. Ker, "The Impact of Gate-Oxide Breakdown on Common-Source Amplifiers with Diode-Connected Active Load in Low-Voltage CMOS Processes," in IEEE Transactions on Electron Devices, vol. 54, no. 11, pp. 2860-2870, Nov. 2007, doi: 10.1109/TED.2007.906938.
3. W. Lim et al., "Dual-Mode CMOS Power Amplifier Based on Load-Impedance Modulation," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 11, pp. 1041-1043, Nov. 2018, doi: 10.1109/LMWC.2018.2871339.
4. Y. Jin and S. Hong, "A 24-GHz CMOS Power Amplifier with Dynamic Feedback and Adaptive Bias Controls," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 2, pp. 153-156, Feb. 2021, doi: 10.1109/LMWC.2020.3038041.
5. G. Luong, E. Kerhervé, J. -M. Pham and P. Medrel, "A 2.5-GHz Multimode Broadband Bias-Segmented Power Amplifier with Linearity-Efficiency Tradeoff," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 11, pp. 1038-1040, Nov. 2018, doi: 10.1109/LMWC.2018.2869600.
6. D. Parveg, M. Varonen, D. Karaca, A. Vahdati, M. Kantanen and K. A. I. Halonen, "Design of a D-Band CMOS Amplifier Utilizing Coupled Slow-Wave Coplanar Waveguides," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 3, pp. 1359-1373, March 2018, doi: 10.1109/TMTT.2017.2777976.
7. Meaamar, A., Chirn Chye Boon, Kiat Seng Yeo, & Manh Anh Do. (2010). A Wideband Low Power Low-Noise Amplifier in CMOS Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 57(4), 773–782.
8. S. M. S. Rashid, A. Roy, S. N. Ali and A. B. M. H. Rashid, "Design of a 21 GHz UWB differential low noise amplifier using .13μm CMOS process," Proceedings of the 2009 12th International Symposium on Integrated Circuits, 2009, pp. 538-541.
9. R. Fiorelli, A. Villegas, E. Peralías, D. Vázquez and A. Rueda, "2.4-GHz single-ended input low-power low-voltage active front-end for ZigBee applications in 90 nm CMOS," 2011 20th European Conference on Circuit Theory and Design (ECCTD), 2011, pp. 829-832, doi: 10.1109/ECCTD.2011.6043831.
10. D. Linten et al., "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS," in IEEE Journal of Solid-State Circuits, vol. 40, no. 7, pp. 1434-1442, July 2005, doi: 10.1109/JSSC.2005.847490.
11. W. Yang, D. Kelly, I. Mehr, M. T. Sayuk and L. Singer (2001), A 3V 340mW 14b 75 Msample/s CMOS ADC with 85dB SFDR at Nyquist Input, IEEE Journal of Solid-State Circuits, 1931-1936, (Vol. 36). https://doi.org/10.1109/4.972143
12. S. Ardalan and J. Paulos (1987), An analysis of nonlinear behavior in delta - sigma modulators, in IEEE Transactions on Circuits and

Systems, S. Ardalan and J. Paulos, An analysis of nonlinear behavior in delta - sigma modulators, in IEEE Transactions on Circuits and Systems, 593-603, (Vol. 34). https://doi.org/10.1109/TCS.1987.1086187

13. S. R. Norsworthy, R. Schreier and G. C.Temes (1996), Delta Sigma data converters: Theory, Design and Simulation, New York, IEEE press.
14. N. Mukahar and S. H. Ruslan (2012), A 93.36 dB, 161 MHz CMOS Operational Transconductance Amplifier (OTA) for a 16 Bit Pipeline Analog to Digital Converter (ADC),International Journal of Electrical and Computer Engineering (IJECE), 106-111, (Vol. 2).
15. M. Marufuzzaman, S. Z. Abidin, M. B. I. Reaz and L. F. Rahman (2014), Design of 3 bit ADC in 0.18µm CMOS Process, Telkomnika Indonesian Journal of Electrical Engineering, 5197-5203, (Vol. 12). http://doi.org/10.11591/tijee.v12i7.3618
16. Y. Fan, Y. Huijing and L. Gang (2013), A High Performance Sigma-Delta ADC for Audio Decoder Chip,Telkomnika, 6570-6576, (Vol. 11). http://dx.doi.org/10.11591/telkomnika.v11i11.3498
17. S. H. Ardalan and J. J. Paulos (1987), An analysis of nonlinear behaviour in delta sigma modulator, IEEE Trans. circuits and sys., 593-603, (Vol. 34). https://doi.org/10.1109/TCS.1987.1086187
18. R. Thankachan, K. R Jayakrishnan and T. K Shahana (2015), Design of 1 bit DAC for delta sigma modulator, Conference nternational on Emerging Trends in Technology and Applied Sciences, 19-22.
19. B. Razavi (1998), Design of CMOS Analog Integrated Circuits, McGraw Hill, California.
20. S. Chakraborty, A. Pandey, S. K. Saw and V. Nath (2015), A 6nW CMOS operational amplifier for bio- medical and sensor applications, Global Conference on Communication Technologies (GCCT), Thuckalay, 242-245. doi: 10.1109/GCCT.2015.7342659.

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