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Comparative Analysis of Silicon and MoS_2 based Tunnel Field-Effect Transistor

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ABSTRACT
Molybdenum Disulfide (MoS_2) is the area of attention due to its wide variety of potential in electrical and optoelectronic devices. High-performance transistors may use nanomaterials in the future. In this paper, we have reported a comparison study MoS_2 based TFET and Silicon-based tunnel field-effect transistor (TFET) structures with a channel length of 10 nm. The step structure has been used for both the device to increase the tunneling as the energy gap varies with the number of MoS_2 layers. In step structured devices, the MoS_2 based TFET has shown better V_{th}, Subthreshold Swing (SS), and I_{ON}/I_{OFF} ratio values that are 0.39V, 7.09 mV/decade and 10^{13}, respectively. The comparison of two simulated devices has been done on based of transfer characteristics, energy band diagram, output characteristics, potential filed, electric field and BTBT rate.

KEYWORDS
Molybdenum Disulfide (MoS_2), Silicon; Step Structure; Tunnel Field-Effect Transistor (TFET)

1. INTRODUCTION

In the semiconductor industry, the transistor is the fundamental unit utilised to construct any electronic circuits and systems. The transistors can be divided into two categories: Bipolar Junction Transistor (BJT) [1] and Field-effect Transistor (FET) [2]. Moore's law says that the number of transistors will double every two years on electronic chips. This means that traditional transistors will get smaller so that high-performance, low-power devices can be made [3]. Traditional metal-oxide field-effect transistors (MOSFET) continue to shrink in size, causing the semiconductor industry to operate with 14nm technology for the next fifty years. When the gate voltage is turned off, a transistor with a small channel length begins to experience high current flow, which is known as off-state current. Off current and drain voltage create greater static power dissipation, which raises the temperature and reduces reliability. The two main causes of power dissipations in transistors are an increase in static power and current leakage. Short channel effects are problems that transistors encounter because of this power dissipation [4]. Scientists have invented novel devices including multi-gate transistors [4], ultrathin body (UTB) transistors [5], Fin-Field-Effect Transistors (FinFETs), and TFETs to reduce Short Channel effects (TFETs) [6]. A field-effect transistor with more than one gate is referred to as a multi-gate transistor. When the bulk transistor is reduced in size using 90nm technology to get better performance, researchers suggest new devices called UTB transistors. The subthreshold leakage current in UTB transistors can be reduced, however with technology below 45nm, the DIBL field fringe has been observed [7-8].

2-Dimensional (2D) materials can contribute significantly to the development of high-performance electronic devices [9]. The carriers have tremendous mobility because the 2D material is "quantum-confined" in the third dimension. They are used in transistors because of their high mobility, which is an attractive attribute to researchers. Crystalline and referred to as single-layer materials, 2D materials are made up of just one or a few atomic layers [9-10]. Strong covalent bonds exist between the atoms in a single atomic layer, whereas the van der Waals (vdWs) interaction across layers is low [11-14]. Graphene and Metal Dichalcogenide (MX_2) are the two materials that are currently attracting the attention of researchers due to their expanding properties in 2D materials [15]. Graphene nanoplates, nanosheets, and nano disks are a few examples of 2D materials made of carbon-based components [16-17].

An innovative Thickness Engineered Tunnel FET based on 2D materials was proposed by P. Kaushal et al. [18]. The device has been modified to increase I_{ON} current by using the effect of channel layer thickness change on bandgap. Also, the analog/RF parameters have been explored for the proposed device. Black phosphorus TFETs with thickness control for low power switches have been suggested by S. Kim et al [19]. Black phosphorus was used in this device for the source region as well as for channel region. To study the unique characteristic of MoS_2 material known as energy bandgaps that vary on layer thickness, F. W. Chen et al. [20] developed phosphorene, which is a 2D material, based Thickness Engineered TFET).

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For the very first time, the comparison of the thickness engineered silicon based TFET and MoS_2 based TFET has been reported in this paper. In this article section II describes the specification of simulated devices. Results and performance analysis of the simulated device are presented in Section III based on the transfer and output characteristics, band diagram, potential field distribution, electric field distribution and band-to-band tunneling (BTBT) rate. Section IV discusses the conclusion of the article.

2. SPECIFICATION OF SIMULATED DEVICES

The 2D cross section view of Silicon based TFET and MoS_2 based TFET are illustrated in Fig. 1. First, the Atomistic Toolkit (ATK) Density Functional Theory (DFT) approach was used to perform first-principle [21]. The widths and concentrations of the carriers vary between the source and drain sections of the designs. The simulated devices have channel length of 10nm which is having two thickness values i.e., channel thickness of 15 nm from 20nm to 25nm and a channel width of 5 nm from 25nm to 30nm length, enabling thickness engineering along the channel. Doping concentrations were 1×10^{20} cm^{-3} for the source (P+ type) and 1×10^{18} cm^{-3} for the drain (N+ type). The concentration for channel doping is 1×10^{12} cm^{3}. Both top and bottom gates have been constructed using the HfO_2 material as the dielectric. Near the source end, 1 nm of oxide thickness is used. The use of HfO_2 as a gate dielectric material has improved coupling between the gate and tunnel junction, which is reflected in an increase in SS and ON current. Gate metal has been made from aluminum. Table 1 is a summary of all the device parameters for the simulated devices.

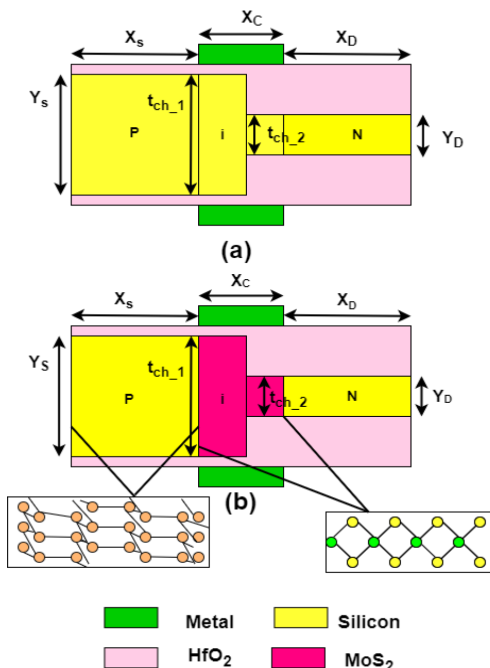


Fig. 1 2D cross section view of (a) Silicon based TFET, (b) MoS_2 based TFET.

Table. 1 Design parameters of simulated devices.

Design Parameters	Notation	Units	Si based TFET	MoS_2 based TFET
Channel length	X_{ch}	nm	10	10
Source Length	X_s	nm	20	20
Drain Length	X_d	nm	20	20
Source width	Y_s	nm	15	15
Drain Width	Y_d	nm	5	5
Gate Work Function	Φ	eV	3.9	4.1
Channel thickness 1	t_{ch_1}	nm	15	15
Channel thickness 2	t_{ch_2}	nm	5	5
Channel Doping	N_{ch}	cm^{-3}	1×10^{12}	1×10^{12}
Source Doping (p-type)	N_s	cm^{-3}	1×10^{20}	1×10^{20}
Drain Doping (n-type)	N_d	cm^{-3}	1×10^{18}	1×10^{18}

3. RESULTS AND PERFORMANCE ANALYSIS

In the commercially available TCAD tool, the Silicon-based TFET and the MoS_2-based TFET are compared using 2D numerical simulations (ATLAS). The properties of both the silicon and MoS_2 material is mentioned in Table 2. Appropriate models have been called upon in the simulator to precisely recreate the device's properties. The Lombardi mobility (CVT) model is used in this work to take the impact of concentration and field dependent mobility into consideration. To consider carrier recombination, Shockley Read-Hall (SRH) is used. Band Gap Narrowing (BGN) is the model that is employed to activate the high concentration effect that occurs in the band gap. To account for variations in the characteristics of a strongly doped region, Fermi-Dirac statistics are used. In addition, a non-local BTBT model is employed to simulate the tunneling effect. To validate the performance benefits of the MoS_2-based device over the conventional.

Table. 2 Properties of Silicon and MoS_2 material

Parameter	Silicon [22]	MoS_2 [23]
Bandgap (eV)	1.12	1.29
Electron Mobility (Cm^2/Vs)	1400	825
Hole Mobility (Cm^2/Vs)	450	155
Electron Mass	0.98 m_e	0.47m_e
Hole Mass	0.49 m_e	0.63m_e

The effect of the transfer characteristics for the two TFETs is shown on a logarithmic scale in Fig. 2. It is noted that MoS_2 based TFET produces greater value drain current i.e., 1.89×10^{-6} A/μm. This is because the less scattering in 2D materials as compared to silicon material in the channel. MoS_2 material based TFET has obtained the threshold voltage (V_{th}), SS and I_{ON}/I_{OFF} ratio of value 0.39V, 7.09 mV/decade and 10^{13}, respectively. Additionally, the source-channel junction has an HfO2 oxide layer, which improves gate coupling and raises the probability that the majority charge carrier will tunnel through

the junctions. Furthermore, with the high rate of charge carrier tunneling, MoS_2 based TFET has low ambipolar current as compared to Silicon based TFET.

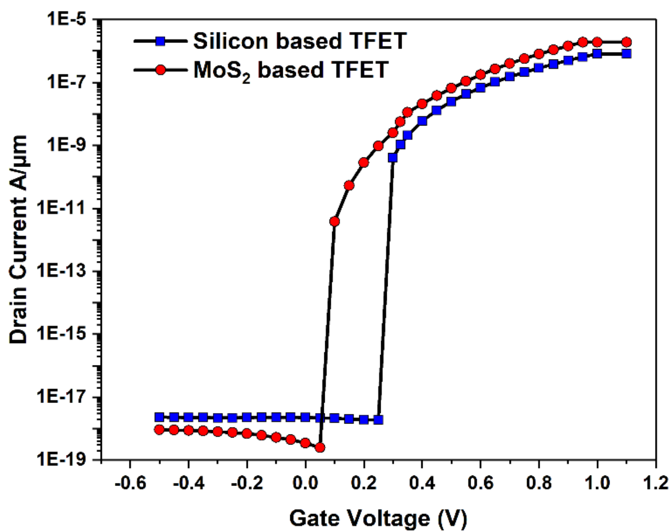
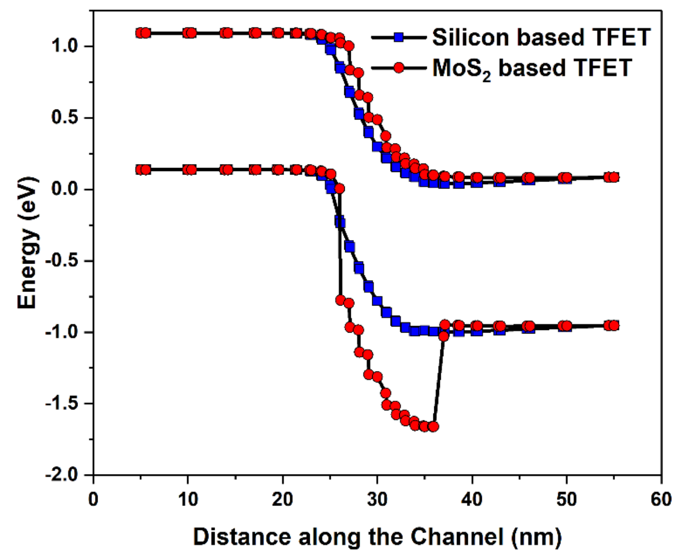


Fig. 2 Transfer characteristics comparison of silicon based-TFET and MoS_2 based TFET.

Fig. 3(a) displays the energy band diagram in the OFF state (V_{gs} = 0V, V_{ds} = 0V). There is no energy band overlap, as a result, the electron is unable to tunnel from source region to channel region, turning the device off. The energy band diagram for the ON (V_{gs} = 1V, V_{ds} = 1V) state has been shown in Fig. 3(b). The tunneling width near the source and channel interface begins to decrease hence, the tunneling rate rises as the gate voltage rises. The figure shows that the MoS_2 based TFET has greater carrier tunneling because the tunneling width is smaller.

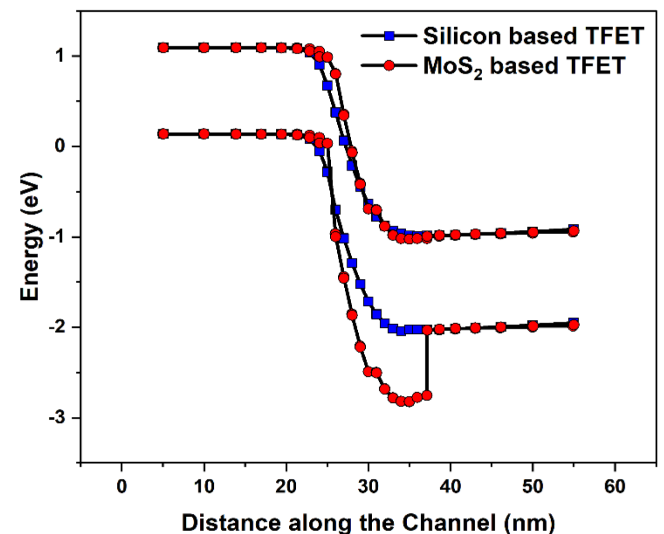
In Fig. 4, The output characteristics (I_d-V_{ds}) of two simulated devices with a 10nm channel length as determined by simulation analysis are shown. Observing the drain current of the device while holding V_{ds} constant and adjusting V_{gs} yielded the output characteristics. For the TFETs made of silicon, the characteristics at V_{gs} = 0.5V, 1V, and 1.5V are shown in Fig. 5(a). For both the considered devices, the drain current has increased along with an increase in V_{gs}. The device using MoS_2 channel material has attained the drain current, which is around 10^{-5} A/m, as shown in Fig. 5 for V_{gs} = 1.5V. The drain current range for V_{gs} equal to 0.5V and 1V is 10^{-7} A/m and 10^{-6} A/m, respectively. For MoS_2 material based TFET the drain current gets saturation earlier than silicon-based device, which shows that the gate has a good electrostatic hold on the channel.

Fig. 5(a) shows the potential field diagram throughout length of the channel of the devices. In the TFET devices, steeper the potential at source channel interface i.e., started at 20nm of the device where channel started, the carrier tunneling is large. Fig. 5(b) shows the electric field diagrams for the two simulated TFET structures when they are turned ON. Since the tunnelling rate depends on the electric field, the stronger electric field causes a greater



band to

(a)

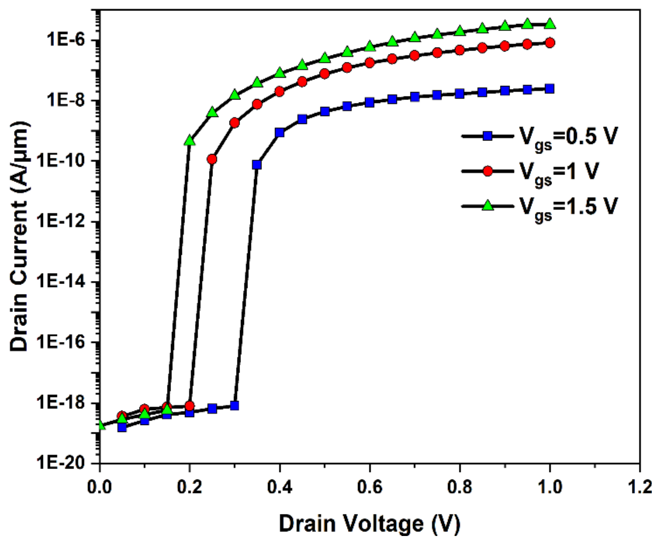


(b)

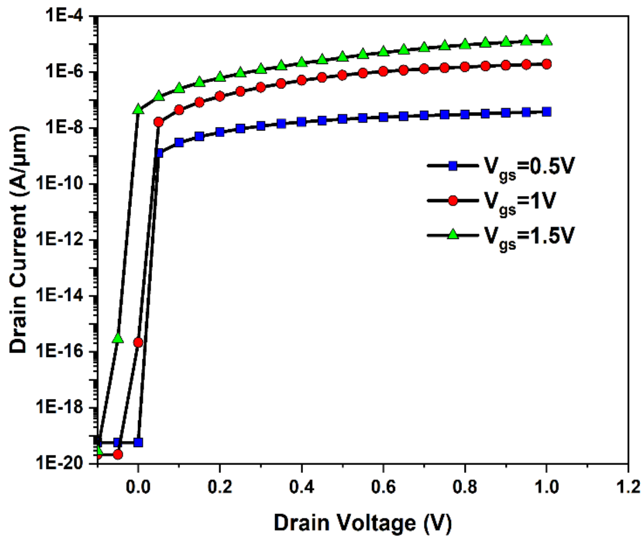
Fig. 3 (a) Energy band profile at OFF-State i.e. V_{gs}=0V and V_{ds}=0V (b) Electric field profile at ON-State i.e. V_{gs}=1 V, V_{ds} = 1 V.

band tunnelling rate for electrons to tunnel. It is shown that the maximum overshoot of electric field, MoS_2 based TFET (4.49×10^6 V/µm) is larger than Silicon based TFET. Because the MoS_2 based TFET has a higher peak electric field, it has a higher drain current than a silicon based TFET.

Fig. 6 has shown the BTBT rate of the device. The BTBT rate refers to the rate at which the carrier transitions from source region to channel region. The MoS_2 based TFET has a greater BTBT rate, which indicates more charge carrier tunneling and therefore more current in the device, according to Fig. 6. Table 3 shows the comparative analysis of simulated devices with some references. The comparison based on SS, V_{th}, I_{OFF} and I_{ON} performance parameters.



(a)

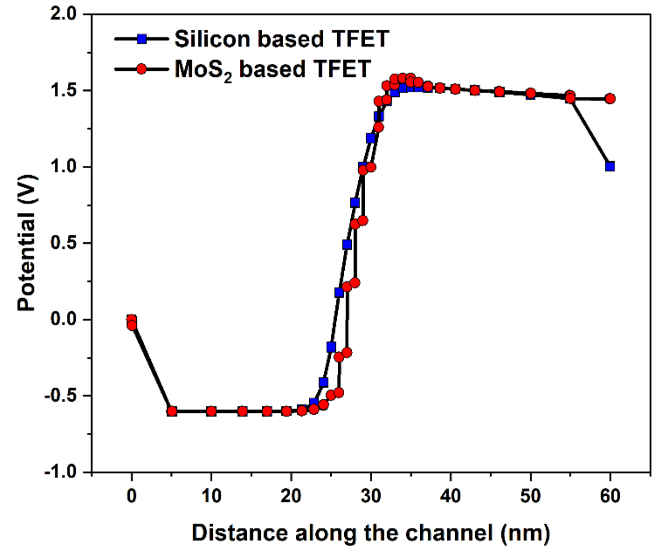


(b)

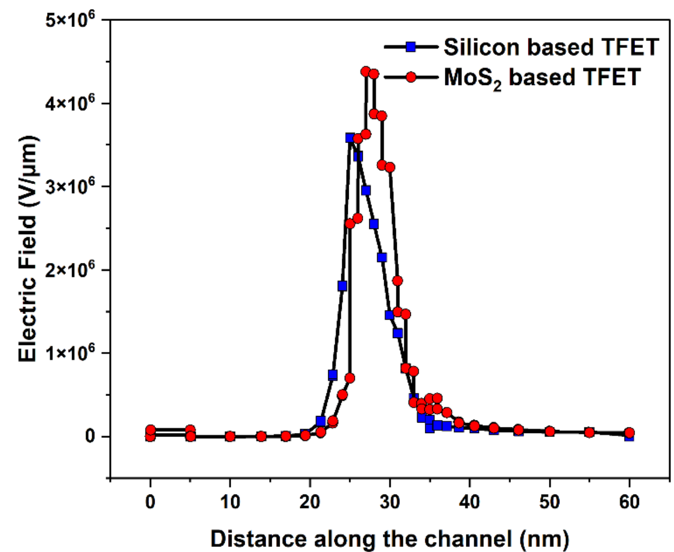
Fig. 4 Output characteristics for (a) Silicon based TFET (b) MoS_2 based TFET at V_{gs} = 0.5 V, 1 V and 1.5 V.

4. CONCLUSION

To address the drawbacks of Silicon-based TFET, this research presents a TFET that is based on MoS_2 Channel material. The comparative analysis of the devices is shown by transfer characteristics, energy band diagram, output characteristics, potential filed, electric field and BTBT rate. The proposed device employed combines benefits of both step-structured and energy gap variation with number of layers increases in MoS_2 material which result in low V_{th}, high I_{ON} in the order 10^{-6} A/μm with 7.09 mV/decade SS. In addition to it I_{ON}/I_{OFF} ratio in the order of 10^{13}. This makes a very promising device for digital circuit applications. These results prove that MoS_2 based TFET is suitable for low power electronic devices.



(a)



(b)

Fig. 5 (a) Potential Field and (b) Electric Field of simulated devices.

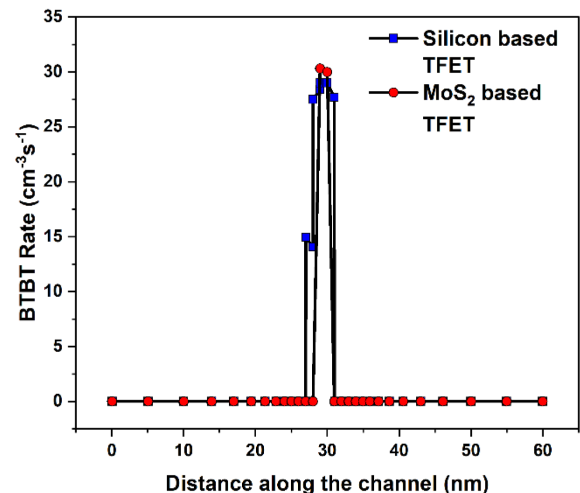


Fig. 6 Comparison of BTBT Rate.

Table. 3 Comparative Analysis

Device	SS (mV/decade)	V_{th} (V)	I_{OFF} (A/µm)	I_{ON} (A/µm)
MoS_2 based TFET	13.59	0.391	3.45×10^{-19}	1.89×10^{-06}
Silicon based TFET	22.07	0.43	1.99×10^{-18}	8.09×10^{-07}
Ref [24]	36.88	0.29	3.79×10^{-13}	2.95×10^{-05}
Ref [25]	52	-	1.165×10^{-17}	2.08×10^{-08}
Ref [26]	-	-	$\sim10^{-13}$	$\sim10^{-7}$
Ref [27]	23.75	0.37	$\sim10^{-17}$	$\sim10^{-6}$
Ref [28]	-	-	6.59×10^{-13}	3.18×10^{-05}
Ref [29]	-	-	6.15×10^{-15}	3.12×10^{-04}
Ref [30]	-	-	3.12×10^{-11}	4.70×10^{-05}

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Contributions: Writing-review & editing, Visualization, Validation, Supervision, Resources.

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