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A High-Performance Miniature 8.2 GHz Band Pass Filter Using Multilayer IPD Inductor for UWB and 5G Radio

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ABSTRACT

This paper describes the simulation and fabrication of a miniature onchip Bandpass Filter (BPF) using the Integrated Passives Device (IPD) process for UWB and 5G Radio Frequency Front End (RFFE) solutions. Technology driven miniaturization led to regular geometry shrinking for components and ICs also. A novel high quality series stacked double_split path inductor is developed with minimum onchip area. The proposed novel double_split (2_split) IPD inductor showed excellent improvements of 53.2% and 36.67% of inductance and quality factor respectively, against the nearest matching inductor in Table 1. A planar high performance spiral capacitor is modeled to design a simple low cost first order LC resonator BPF circuit. The 8.2 GHz BPF simulated using High Frequency Simulation Software (HFSS), yielded very good performance enhancements: Q factor of 13.68, smaller 7.31% fractional bandwidth, very low -0.25 dB insertion loss, -26 dB return loss and finally very small chip space of only 0.144 mm2. This proposed IPD BPF demonstrated very narrow bandwidth, yet occupying least possible footprint. These IPD passives are fabricated by scaling down to mm scale due to PCB fabrication difficulty at nm scale. The mm level downscaled and fabricated LC resonator BPF is tested on Agilent network analyzer (VNA-N9923A). The PCB measured results of the BPF are in very good concurrence with simulation results. The proposed compact 8.2 GHz BPF performance is validated from above successful results. All these superior parameter enhancements clearly prove that the proposed 8.2 GHz BPF using the novel 2_split inductor, is highly suitable for Radio Frequency Integrated Circuit (RFIC) applications at 8 GHz UWB band.

KEYWORDS

BPF; HFSS; Insertion Loss; IPD; Multilayer; Quality factor; RFFE

1. INTRODUCTION

Today's information centric world is witnessing a massive mobile multimedia proliferation, with an explosion of smart mobile devices for wireless communication, navigation and sensing applications. FCC allotted 3.1-10.6 GHz spectrum to enrich mobile multimedia from 5G enhanced mobile broadband (eMBB) to ever growing UWB networking. The latest smartphone brands use an UWB application interface (API). Smart wireless networks need area efficient high quality RFFE circuit components to reduce the size of ICs and devices [1]. In literature, successful RFFE circuits prominently used the low-cost high-performance CMOS process integrated with small sized IPD process [2]. On chip Passive components are indispensable beyond 1 GHz due to their noise and power advantages. On chip inductor is the basic passive element in the CMOS RFIC. Typical smart phone architectures require about 30 onchip passive capacitors and inductors occupying large RFIC chip area of ~ 70%. LTCC filters reported smaller losses but with in-creased size and heat problems [3, 4]. Microwave resonators possess low loss responses, but have large complexity and bigger size. MEMS integrated devices were produced with low loss, small size components. But they consume large power and have instability [5]. The IPD technology favor miniature integrated onchip passives to develop high quality RFICs for the UWB and 5G system on chip (SOC) applications.

The IPD based RF circuits become prominent at present to implement key RF performers like BPFs, LNAs, etc. in a SiP [6]. Many RFFE circuits are successfully developed on low cost Si CMOS technology using the low loss IPD onchip passives, to produce an SOC [7]. A compact 3.6 GHz WIMAX RF BPF implemented using Silicon IPD showed attenuation of 40 dB but occupied large area of 1.92 mm2 [8]. An IPD dual band glass substrate 4.8 GHz BPF reported 2.5 dB S12 value with a chip pace of 0.9 mm2 [9]. A Si IPD UWB filter designed for 2.9-9.4 GHz band showed S12 value of 0.4 dB with a large space of 6.96 mm2 [10]. A triple-mode UWB filter with 3.1-10.6 GHz passband is realized with 13 dB return loss but occupied huge area of 177 mm2 [11]. An IPD BPF at 3.5 GHz showed -1.6 dB insertion loss with an occupied chip space of 1.28 mm2 [12]. A miniature 3.3-5.8 GHz 5G BPF using stepped impedance resonators reported 1.5 dB insertion loss, 20 dB return loss but suffer large area of 121 mm2 [13]. A glass IPD 5G BPF for n77 band showed 1.4 dB insertion with 2.5 mm2 area [14]. A HRS IPD based 5.48-8.29 GHz 5G n77 BPF reported 1.76 insertion loss, 30 dB return loss and large area of 2.5 mm2 [15]. A multi-mode resonator 5G BPF reported 18 dB return loss but had large 2.5 dB insertion loss [16]. A GaAs IPD BPF showed S12 of 3 dB and S11 of 15 dB having area of 1.135 mm2 [17].An 8 GHz SAW BPF had 13.2 dB insertion loss with 2.25 mm2 area [18]. It is observed from the above works that, the square spiral structures can reduce the onchip area occupied by passive elements.

Thus, the design and simulation of miniature IPD passives and a high quality BPF is proposed to meet the stringent spectral needs of 5G RFICs. This paper reports on the design of a novel three-layer double_split spiral inductor and a planar capacitor to demonstrate a low cost miniaturized first order LC resonator BPF. Corresponding BPF is also fabricated on FR4 substrate PCB to test and validate the high performance of pro-posed BPF employing IPD passives. This paper is comprised the sections 2, 3 and 4 as reported.

2. DESIGN AND ANALYSIS OF 8.2 GHZ BPF

The presented BPF is simulated using a novel double_split multilayer IPD spiral inductor and a single layer capacitor. Square geometry is employed as it possess uniform distribution of current with easier fabrication. The 3 layer split inductor structure is a vertical stack of – large substrate (Si), dielectric in between and 3 metal top layers. The metal surface, bond, test and lead layers enable very concise model. The dielectric layer (SiO2) is placed in between the top copper metal layer and 0.2 μm thick gold metal vias on very thick Substrate.

2.1 On Chip Multilayer Inductor

Simple, approximate inductance expressions for spiral inductors of different geometries were derived in past using Greenhouse, modified Wheeler, Current sheet and data fitting methods. Typical inductor tolerance value is of several percent order, relaxing the necessity of "more accurate" expressions in practice [19]. Onchip inductors with line width variation yielded higher quality factors [20]. The net inductance of a spiral inductor is the sum of its self inductance, positive and negative mutual inductances of a spiral structure [21]. Consider a typical three turn spiral inductor which has 12 conductor segments as indicated in the Fig. 1.

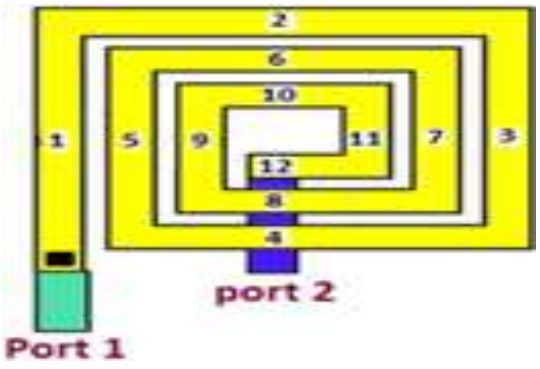

Fig. 1. A typical three turn square shaped spiral inductor with inductances indicated

The expression for its self-inductance is given by [5]

$$L_{self} = 0.2\mu l_i \{ln(\frac{2l_i}{w+t}) + 0.5 + (\frac{w+t}{3l_i})\} \quad (1)$$

Where li is the ith segment conductor length, w and t are conductor width and thickness and μ is permeability of conductor metal. Total self-inductance for spiral inductor is thus

$$L_{self} = \sum_{i=1}^{12} L_i \quad (2)$$

Mutual inductance between any two adjacent segments is same with Mi,j=Mj,i. Positive and negative mutual inductances for the three turn spiral inductor are [5].

$$M_{+ve} = 2(M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,11} + M_{3,7} + M_{4,8} + M_{4,12} + M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}) \quad (3)$$

$$M_{-ve} = 2(M_{1,3} + M_{1,7} + M_{1,11} + M_{5,11} + M_{5,3} + M_{5,7} + M_{9,3} + M_{9,7} + M_{9,11} + M_{2,12} + M_{2,4} + M_{2,8} + M_{9,3} + M_{9,7} + M_{9,11} + M_{2,12} + M_{2,4} + M_{2,8}) \quad (4)$$

Hence, the overall inductance is

$$L_{Total} = L_{Self} + \sum M_{+ve} + \sum M_{-ve} \quad (5)$$

The analytical evaluation to extract the impedance value of a spiral inductance is quite complex and cumbersome, so as to solve field expressions [29]. Much simpler yet accurate method is to find the inductance from the Y parameters, which are found through S parameters obtained in HFSS simulation model of a spiral inductor structure [21]. Inductance and Q factor are computed as

$$L = \frac{-1}{2\pi \times f_0 \times Im[Y_{11}]} \qquad Q = \frac{Im[Y_{11}]}{Re[Y_{11}]} \quad (6)$$

The Q factor for inductor is found by

$$Q = \frac{\omega L_s}{R_s \left(1 + \frac{R_s}{R_p\{(\frac{\omega L_s}{R_s})^2 + 1\}}\right)} [1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p)] \quad (7)$$

Previous Si based designs for onchip inductors, indicate a maximum Q value around 10-15 with large occupied chip spaces. Multiturn series stacked IPD inductor geometry enhanced the Q value, inductance L, and self resonant frequency fSRF [22, 23].

The proposed three layer IPD inductor is developed with copper as conductor on a thick silicon substrate. Its outer diameter is 100 μm and the onchip area is 100 μm2. The proposed novelty of splitting the conductor width by 50% throughout the length of conductor, yields large inductance (L), mainly due to increased mutual inductance between the two tracks. This proposed inductor is simulated in HFSS, using a lumped circuit model to obtain values of impedance L and Q factor. These values are validated by comparing them with the values obtained by solving analytical methods Grover method. The planar, 3D and HFSS structures of the proposed IPD inductor is shown in Fig.2.

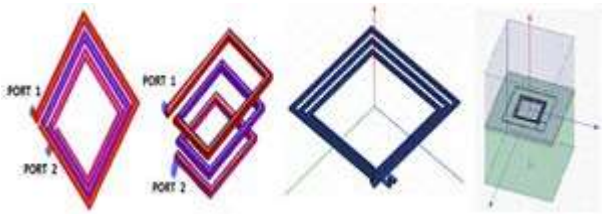

Fig. 2 The planar, 3D, HFSS simulated split inductor and total geometry of the proposed double split 3 layer IPD inductor.

The inductor has one full conductor turn per each layer. The inductance and Q factor (Q) variation are plotted in Figure 3. The dimensions of the onchip inductor: Conductor spacing, thickness and width are 2 µm, 2 µm and 4 µm respectively. The spacing between adjacent layers is 2 µm and the overall occupied area is 100 100 µm2.

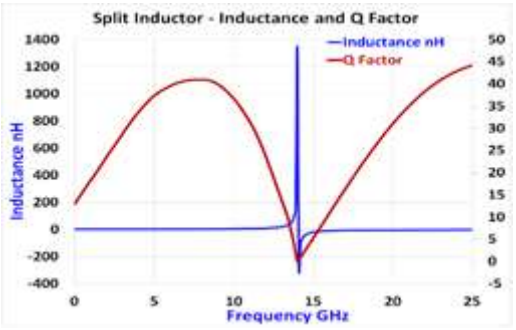

Fig. 3 Inductance Q Factor variation for the proposed Double Split IPD Inductor

The performance of this simulated 180 nm CMOS IPD inductor yielded a higher Q factor of 41 and fSRF of 14.0 GHz. Hence the proposed double_split IPD inductor is proved suitable for 8 GHz UWB and 5G RFIC applications chiefly due to its minimum onchip space.

2.2 Onchip Spiral Capacitor

design, low cost and miniaturization goal. It is simulated in HFSS for 8.2 GHz application. The structure uses copper conductor and Silicon substrate. The conductor turns are placed in one single layer, with constant width. The capacitance (C) and inductance (L) values are influenced by material property, conductor spacing width, length, and also number of conductor turns. Fig. 4 shows the planar views of the onchip spiral capacitor and its responses.

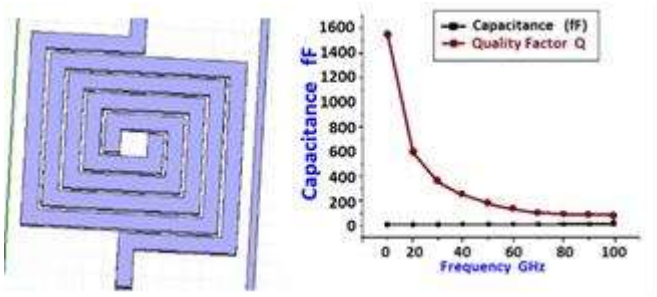

Fig. 4 The planar, HFSS simulated split inductor structures and the performance response of the proposed planar two and half turn IPD Capacitor.

The capacitance C and Q values are found from the S-parameters. Their variations with frequency are depicted in Fig. 4. The dimensions of this two and half turn onchip square capacitor are: Conductor spacing, thickness and width are 1 µm, 2µm and 4 µm respectively.

Table 1. Performance comparison of IPD double split inductor and planar capacitor.

Type of Passive Component	Inductor			Capacitor			SRF GHz
	Inductance nH	Q_L, max	On Chip Area mm^2	Capacitance fF	Q_C	On Chip Area mm^2	
Ref. 3 7 GHz IPD BPF	0.35	-	1.68	2.9	-	0.56	9.0
Ref. 8 7.6 GHz IPD BPF	1.623	30	0.35	7.789	70	0.25	8.36
Ref. 12 5.8 GHz CMOS BPF	0.43	5.5	0.056	3.4	-	0.056	12.5
Proposed 8.2 GHz IPD BPF L C	**2.49**	**41**	**0.01**	**8.46**	**1745**	**0.0025**	**13.5**

The overall occupied area of capacitor is 50 50 µm2. The capacitor had exhibited improvements in the capacitance C and Q factor values. Hence this proposed capacitor is highly suitable component for UWB and 5G

RFIC applications, as it occupied very small area. Table 1 compares the simulation results of proposed 8.2 GHz IPD

inductor and capacitors with the similar onchip passives in literature

2.3 Circuit model and the BPF Resonator

Bandpass filter is the key performance decider for selectivity of any wireless receiver [**28**]. Traditional LTCC/IPD filter technologies, are unable to meet spectral challenges of 5G, 6G and, Wi-Fi 7 [**30**]. It is proposed a simple low cost single stage LC resonator circuit to simulate and implement the proposed IPD BPF at 8.2 GHz. Circuit model and HFSS structure for the LC BPF is given in Figure 4. It consists of the double_split inductor and capacitor forming a LC resonator.

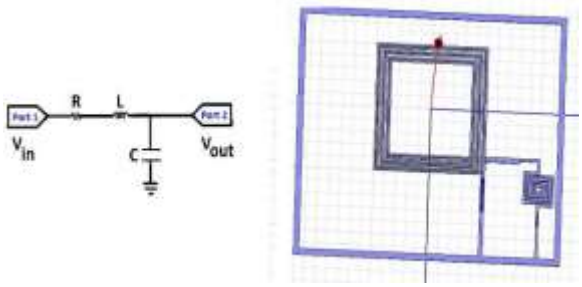

Fig. 5. LC Resonator BPF circuit and HFSS simulated 8.2 GHz BPF.

The BPF simulation is done by replacing the reactive components by the double_split multilayer IPD inductor and the single layer capacitor. The values of L and C are found to be stable in entire passband. Figure 5 shows the proposed series LC filter. The geometry and component optimization was carefully done in HFSS simulations. Figure. 6 shows the two important loss variations for the proposed LC resonant bandpass filter.

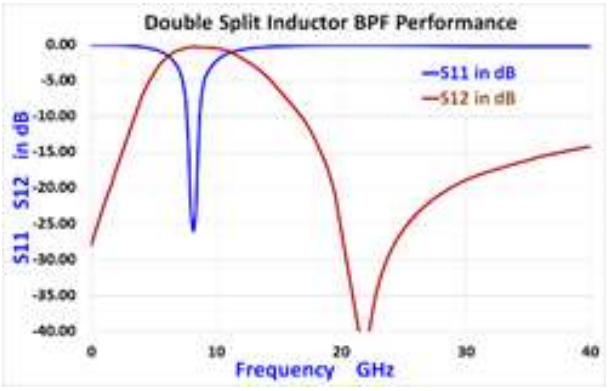

Fig. 6. The simulated loss performance of the proposed 8.2 GHz BPF.

2.4 Simulated Results for the BPF

Proposed double_split inductor produced a Qmax of 41. Similarly, the capacitor showed a Qmax of 1745, as revealed from Figure 2, Figure 3 and Table 1. The proposed 8.2 GHz BPF shows maximum of -26 dB return loss and minimum S21 of -0.25 dB at 8.2 GHz as shown in Figure 5. These excellent results prove the best

performance required by any UWB BPF. The BPF exhibits very narrow 600 MHz bandwidth from 7.85 GHz to 8.35 GHz.

Bandwidth of BPF $\Delta f = (fH-fL) = 0.6$ GHz;

Center Frequency fc = 8.2 GHz

Loaded Q of BPF = $(fc/\Delta f) = 8.2/0.6 = 13.68$

Fractional bandwidth = $\Delta f /fc = 7.31\%$

This superior performance of BPF from the simulation results are summarized in Table 2

Table 2. Summary of the simulated BPF parameters.

8.2 GHz BPF	Design Specifications	Simulation Results
Center Frequency f_c – GHz	8.2	**8.2**
Bandwidth, MHz	500	**600**
Fractional Bandwidth - %	5	**7.31**
Quality Factor, Q	15	**13.68**
Return Loss, S_{11} dB	< -25	**-41**
Insertion Loss, S_{12} dB	< -1	**-0.25**
On Chip Area, mm^2	**< 0.125**	**0.144**

The single stage LC BPF resonator simulated using the proposed novel double_split IPD inductor had produced smallest fractional bandwidth of 7.31%. The excellent insertion loss of -0.25 dB and least return loss of -41 dB will make this BPF to efficiently operate with larger selectivity. It possessed narrow bandwidth and also least occupied onchip space of 0.144 mm2. Therefore, this narrow band response will surely satisfy the 5G BPF spectral response demands. Hence, this proposed 8.2 GHz IPD BPF filter definitely would realize the miniature UWB and 5G RFICs. The performance of the designed 8.2 GHz BPF is compared with similar researched BPFs around 8 GHz in Table 3.

Table 3. Performance comparisons of the designed BPF.

Parameters	f_c GHz	Δf %	Q	S11 dB	S12 dB	On Chip Area mm^2
Ref. 3	8.0	25	4	-10.2	-1.6	15
Ref. 8	7.656	6.89	14.5	-20	-0.3	1.667
Ref. 11	8.0	12	8.3	-33	-0.8	0.394
Ref. 18	6.2	15	6.7	-35	-0.5	452
Ref. 26	6.1	13.6	7.35	-15	-0.6	152.5
Ref. 32	10	54		-18	-3	150

Proposed BPF 2023	**8.2**	**7.31**	**13.68**	**-26**	**- 0.25**	**0.144**

3. RESULTS AND DISCUSSION

3.1 Fabrication of the double split inductor, capacitor and the IPD BPF

The proposed novel double split IPD inductor and planar capacitor are fabricated on a three layer PCB with the low cost FR4 substrate material [24]. Its dielectric constant is 4.4 and the occupied PCB area is 40136 mm2. The thickness of PCB is 1.60 mm with 0.15 mm copper thickness and a metal layer spacing of 0.197 mm.

3.2 Measurement results of the fabricated IPD inductor and Capacitor

Fabrication of small area 180 nm scale inductors and capacitor on a silicon substrate is not available. The only available fabrication facility is a millimeter scale FR4 substrate. Hence technology scaling is done from 180 nm dimension to millimeters, but retaining the structural similarity. So the inductor operating frequency is reduced from 5 GHz to 150 MHz range

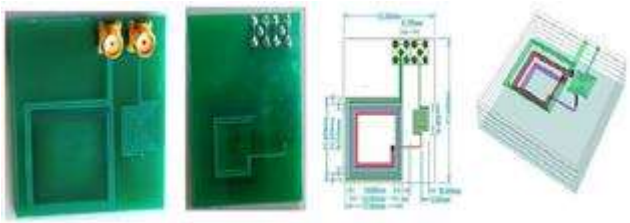

Fig. 7. The PCB, Layout geometry and dimensional details

The fabricated double split IPD inductor, planar capacitor and the BPF layout are shown in Figure 7. Corresponding test setup for experimental measurements is also are shown. Comparison of the measured and simulated values of inductances and Q factors for the novel double_split inductor structure are shown in Figure 8. The two plots clearly indicate that the PCB measurement inductances are in very good matching with simulated inductances about 271 nH with a maximum Q of 53 at 70 MHz with the SRF around 150 MHz

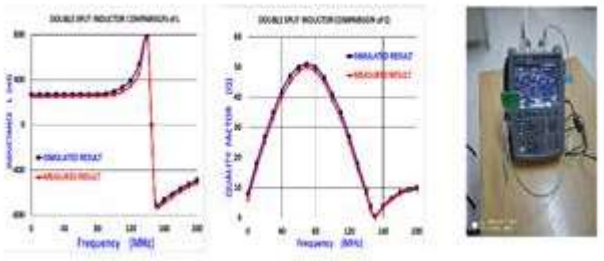

Fig. 8. VNA measurement set up, the simulated and measured results of inductance values and Q factor values for the double_split IPD PCB inductor

Table 4 presents the measured and simulated results for proposed double_split inductors implemented on the three layer PCB. It is well proven that PCB measurement results are in close concurrence with HFSS simulation results. These results prove the supremacy of the proposed novel double_split IPD inductor to realize, an easy to fabricate compact high performance onchip inductors for 5G applications even at 180 nm scale CMOS process.

Table 4. Simulated results vs. measured results for the three layer double_split inductor.

Parameter	*ML Double_Split Inductor*	
	Design Specifications	Simulation Results
SRF f_0 (MHz)	**150**	**153**
Inductance (nH)	**270**	**264**
Q Factor Q	**50**	**48**
Chip Area (mm^2)	**16×16**	**16×16**
Width W (mm)	**2**	**2**
Spacing S (mm)	**1**	**1**

BPF and the measurement results for PCB ML BPF are validated experimentally using the Analyzer VNA-N9923A as shown above. The comparison of HFSS simulated with the PCB Measurement results for the mm level scaled down BPF using the double_split inductor are given in Figure 9 and also in Table 5.

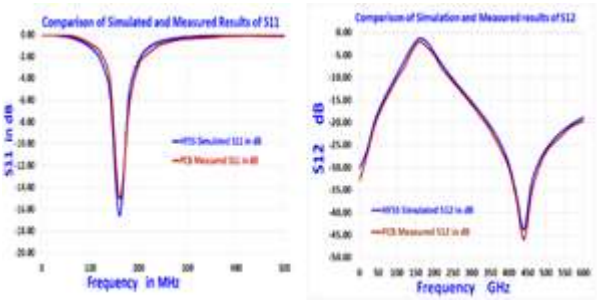

Fig. 9. Simulation and measurement results for the proposed BPF fabricated in mm scale PCB.

Insertion loss deviation between measured and simulated results are due to- the PCB substrate loss tangent inaccuracy and SMA connector losses [31] and test environment error [25].

Table 5. Performance comparison of the simulated and fabricated BPFs.

Parameter	Simulation Results	Measurement Results
S11 - dB	**-16.58**	**-15.86**
S12 - dB	**-1.35**	**-1.89**
Occupied Chip Area - mm^2	**1.6**	**1.6**

The proposed novel double_split multilayer IPD spiral inductor and planar capacitor are designed, fabricated and tested successfully on a three layer PCB. The PCB tested results are in very close agreement with simulation results, demonstrating the superiority of the proposed double_split IPD inductor design [33-37].

4. CONCLUSION

From above results, it can be observed that the simulated results obtained from HFSS simulator and the measured results from VNA analyzer are in good agreement with each other. Hence, based on these excellent findings, the proposed double split IPD inductor simulation results can be validated at 8.2 GHz in 180 nm CMOS process fabrication also. The proposed novelty is to split the conductor width into two equal length tracks (double splitting). This double_split IPD inductor showed excellent improvements of 53% and 36.67% of inductance and quality factor respectively over that of nearest matching inductor in literature. Also the occupied chip space for the proposed IPD inductor is heavily reduced by 3400 times. The proposed planar capacitor design also showed capacitance and quality factor improvements of 8% and 24% respectively over that of nearest matching capacitor in literature. Also the occupied chip space for the proposed IPD capacitor is heavily reduced by 9900 times. Thus, the prime objective the design to obtain highly miniaturized on chip passives is accomplished successfully. The proposed 8.2 GHz IPD BPF demonstrated superior performance in the desired 8 GHz frequency. The proposed BPF demonstrated excellent input matching S11 of 26 dB, very low S12 of -0.25 dB. Finally the BPF occupied a least chip space of 0.144 mm2 only. All such superior parameter enhancements clearly prove that the proposed 8.2 GHz BPF using the novel double_split IPD inductor is promising suitable candidate for the UWB and 5G wireless RF front end application. The objective to design and implement a miniaturized 5G BPF as a high performance RFIC component is achieved successfully.

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