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Design and Analysis of a Low Power Current Starved VCO for ISM band Application

Nikhat Anjum[1], Vimal Kumar Singh Yadav[2], Vijay Nath[1]

[1]Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, India.

[2]Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad, Prayagraj, India.

KEYWORDS

CSVCO; ISM; Low phase noise; Low power; PSS; Ring oscillator; VCO

ABSTRACT

This research paper explores the applications of current starved oscillators in the Industrial, Scientific, and Medical (ISM) band, specifically focusing on the frequency range of 2.4 GHz. Additionally, it examines the challenges and potential future developments in this field. The construction of a 3-stage, 5 stage and 7 stage current-starved CMOS VCO called the Ring oscillator. The size and power requirements of the suggested circuits are extremely low, and they work with wireless technology. The very low power supply 0.9 V is applied. As we vary control voltage its oscillation frequency is also varied. At 2.4 GHz oscillation frequency performance analysis of 3, 5 and 7 stage current starved oscillator is observed. The novelty of proposed work is its better tunning range 0.534 GHz to 11.036 GHz, 0.433 GHz to 6.43 GHz and 0.353 GHz to 4.59 GHz, low power consumption 0.250 mW, 0.254 mW and 0.256 mW and low voltage supply of 0.9 V of 3-stage, 5-stage and 7-stage current starved voltage-controlled oscillator respectively. Phase noise of the 3-Stage, 5-Stage, and 7-Stage CSVCOs at 2.419 GHz was measured at 1 MHz offset to be -75.91 dBC/Hz, -76.38 dBC/Hz, and -79.934 dBC/Hz respectively. PSS analysis found -85.946 dBm, -97.314 dBm and -105.1 dBm of 3, 5 and 7 stage CSVCO respectively at 2.4 GHz frequency. The fragrance of this CSVCO is its low power supply.

1. INTRODUCTION

In the past few decades, wireless communication systems have rapidly evolved and have become an integral part of everyday life. Oscillators play a crucial role as they are the source of most of the communication signals at the receiver side used for the subsequent processing. Various types of oscillators, such as the voltage-controlled oscillator (VCO), are commonly employed in the industrial, scientific, and medical (ISM) band. The ISM band at 2.4 GHz has gained significant importance in wireless communication systems, particularly for applications such as Wi-Fi, Bluetooth, and Zigbee. Current starved oscillators offer several benefits, including low power consumption, high frequency stability, and easy integration. While VCOs offer the benefit of low cost, one of their primary drawbacks is their power consumption due to their high voltage swings. The miniaturization of communication devices demands an oscillator with low power consumption. To meet this requirement, the current starved voltage-controlled oscillator (CSVCO) was proposed. A decrease in frequency is seen as more delay stages are used, however this is accompanied by an increase in generated bias current and power consumption [1]-[2]. Scaling CMOS technology at the 45 nm node and down to fulfil the demands for power, speed, and packing density has continued to be fueled by MOORE'S law [3].

To produce a sinusoidal output signal, each oscillator is made up of an odd number of multi-stage inverters. Only the stages of the delay cell and the voltage supply affect the RO's (Ring Oscillator) output frequency. MOSFETs that are externally biased control the rise and fall times of the cell in the CSVCO. Therefore, one can vary the current supplied to the delay stage by adjusting the size of the MOSFETs, which leads to a decrease in output power and a wider tuning frequency range [4]. The sum of each inverter's stage count and delay gives rise to the oscillator's period. The current, capacitance, and inverter delay can all be controlled. Although capacitance can be changed to see frequency changes with changing transistor length, the current application only supports one stable single channel length, thus the inverter current is changed [5]. The normal range of a linear designed VCO is in GHz [6].

There are two types of Voltage-Controlled Oscillators (VCOs), LC oscillator and ring oscillator. To make sure the Barkhausen conditions are met and to make up for the energy losses of the passive components at each oscillation cycle, LC resonators use a negative resistance component. Low phase noise is a characteristic of these oscillators. They cost money to embed into the chip and take up a significant amount of space. The adjustable ring oscillators make up the other class of VCOs.

Due to the ease with which they may be scaled and integrated in comparison to their competitor, their smaller footprint is appealing [7].In this paper we have designed CMOS ring oscillator, 3-stage, 5-stage, 7-stage current starved voltage-controlled oscillator by using cadence virtuoso gpdk045nm CMOS technology.

We give a quick overview of the CMOS ring oscillator design in Section 2. Section 3 presents the design concept for 3-stage, 5-stage, and 7-stage current starved ring VCOs. Section 4 presents the results of simulations, and Section 5 wraps up this paper's findings.

2. CMOS RING OSCILLATOR

An oscillator is an amplifier with a signal source of its own. An oscillator's principal function is to produce a predetermined waveform at a consistent peak amplitude, at a predetermined frequency, and to hold it within predetermined amplitude and frequency bounds. The simplest CMOS ring oscillators use a chain of odd numbers of single ended inverters [8]. The output of the N^{th} stage is fed back into the input of the first stage. There are no stable operating point exits because of the odd number of inversions in the ring oscillator [9]. The oscillation must satisfy the barkhausen criterion and each stage must add 180°/N phase. Figure 1 (a) depicts the block diagram of an N-stage (N = odd, >1) ring VCO, Figure 1 (b), shows CMOS Inverter based ring oscillator.

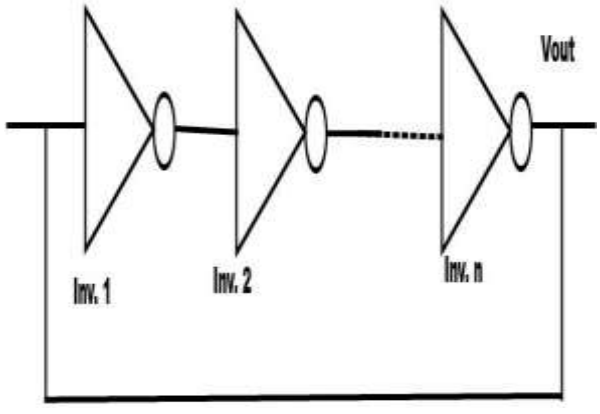


Fig. 1 (a) N stage inverter-based Ring oscillator [10, 36].

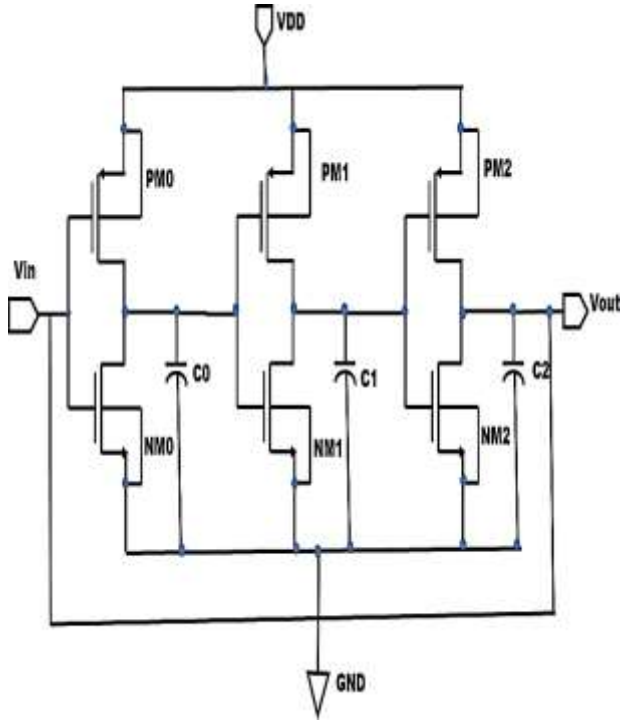


Fig. 1 (b) CMOS Inverter based Ring oscillator [5]

The period of the ring oscillator is determined by the propagation time (t_d) of the signal transition over the entire chain [11]. Which is given by equation (1) as

$$T = 2 * N * td \quad (1)$$

N stands for the chain's total number of inverters (delay stages).

A full cycle necessitates transitions from low to high and from high to low, which leads to factor 2. Only for the conditions $2Nt_d >> t_f + t_r$ where t_r and t_f are the rising and fall time periods, is equation (1) true. Consequently, the oscillation frequency can be written as like equation (2)

$$fo = \frac{1}{T} = \frac{1}{2*N*td} \quad (2)$$

Therefore, by adjusting each stage's time delay, an N-stage ring oscillator's oscillation frequency can be adjusted [12-14].

3. CURRENT STARVED RING VCO

The current-starved oscillator is a well-liked oscillator among conventional voltage-controlled oscillators (VCOs) in various applications [15]. Figure 2 depicts the current-starved oscillator. It functions in a manner akin to the ring oscillator. While MOSFETs P1 and N1 function as current sources, MOSFETs P2 and N0 act as an inverter. The current available to the inverter P2 and N0 is constrained by the current sources IDP1 and IDN1, which are equal to ID. Because of the input control voltage, MOSFETs P0 and N2 have identical drain currents. Each inverter current source stage mirrors the currents in P0 and N2 [16].Controlling is an important component of every system or equipment [19]. Seven inverters, PUN, and PDN cascaded together when constructing the CS-VCO architecture [20]. The PDN network is created using NMOS transistors, while the PUN network is composed of PMOS-

connected load [21]-[25]. One switch, VC, has been integrated into the NMOS transistor's gate to control the frequency. The controlled voltage V fluctuates between 0.3 and 1.2 V, while the Power Supply voltage is 0.9V. Design parameters are given in Table. 1. Figure 2 depicts the schematic diagram for the N-Stage CS-VCO.

Table. 1 Design Parameters of CSVCO

Parameter	Value
Current source PMOS width	3.96 µm
Current source NMOS width	1.98 µm
PMOS width in Inverter	960 nm
NMOS width in Inverter	460 nm

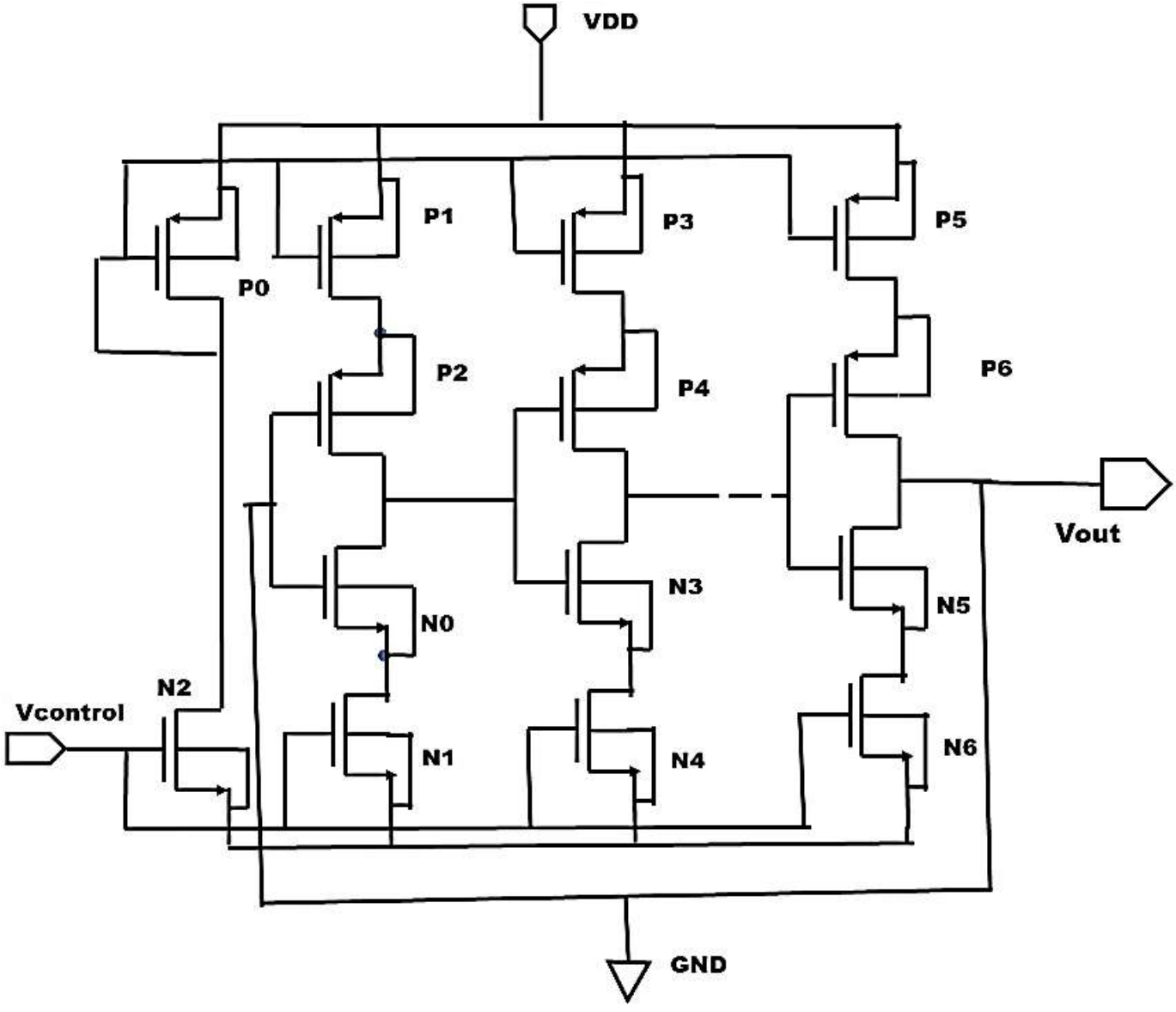


Fig.2 N- stage CSVCO [11]

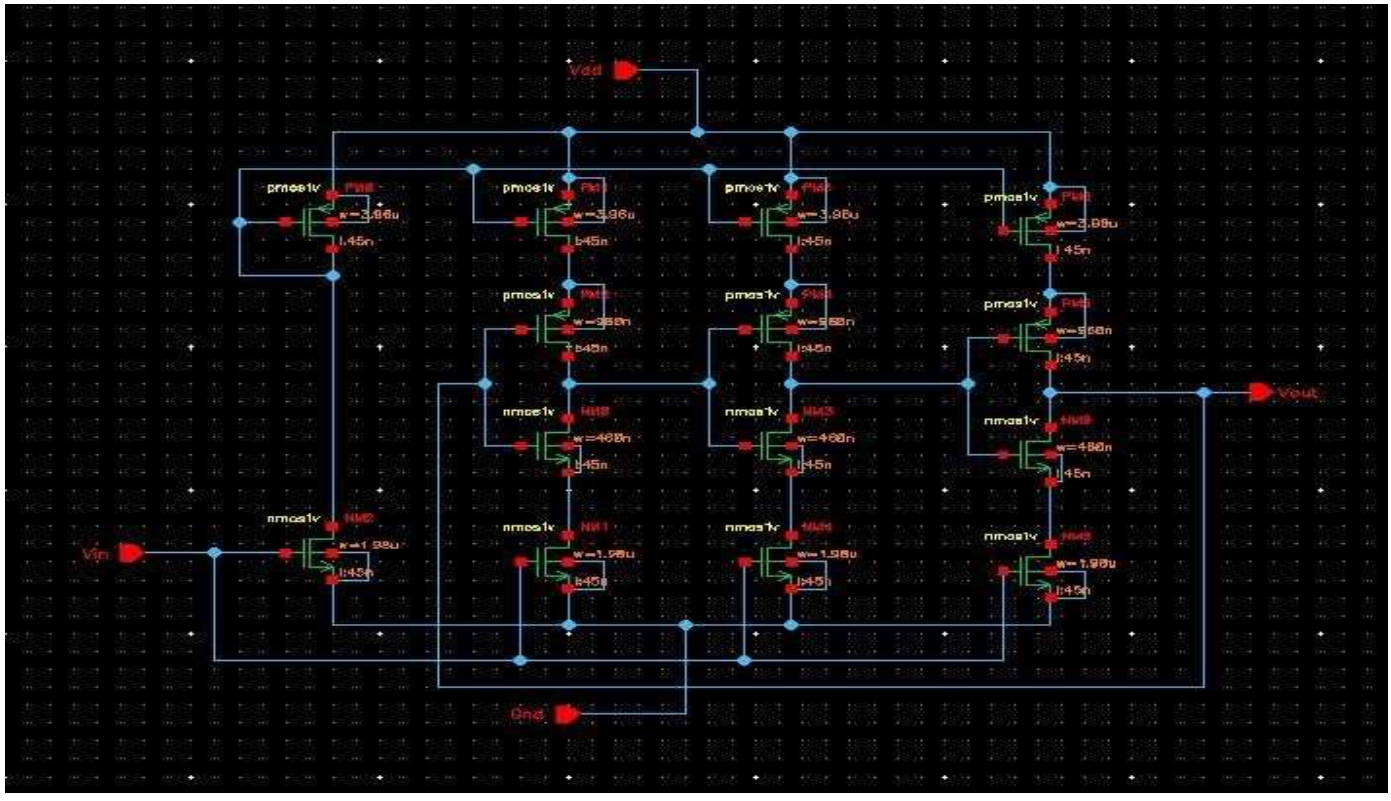


Fig.3 3-stage CSVCO

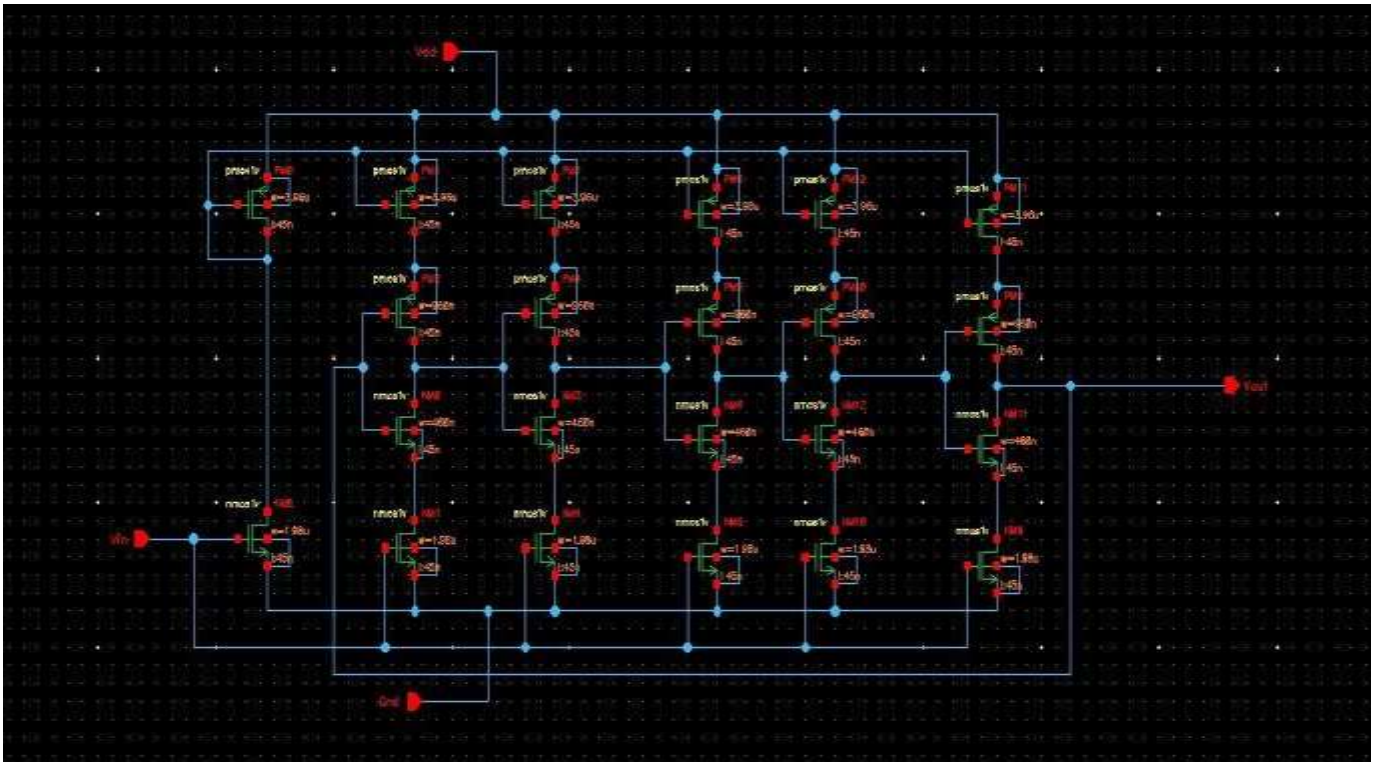


Fig.4 5-stage CSVCO

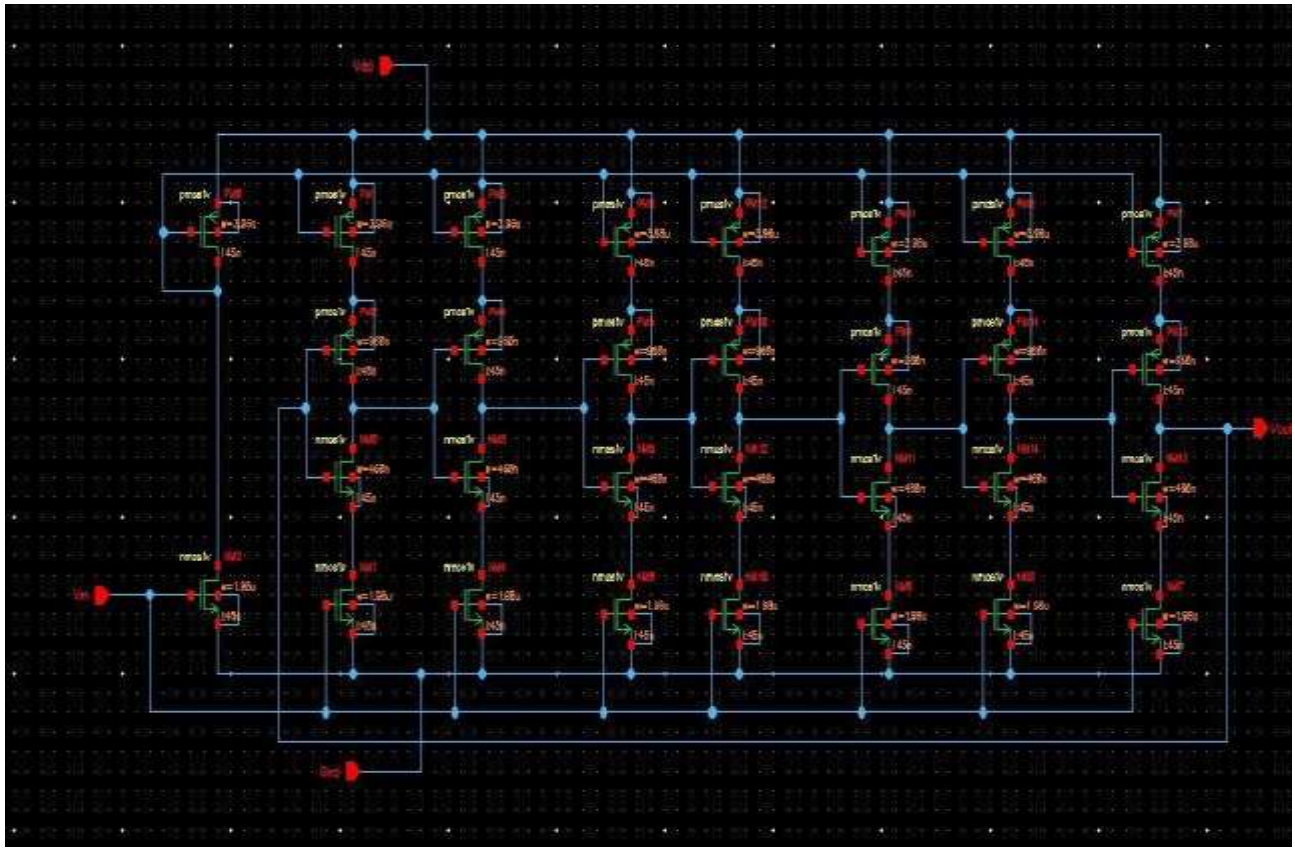


Fig.5 7- stage current starved VCO

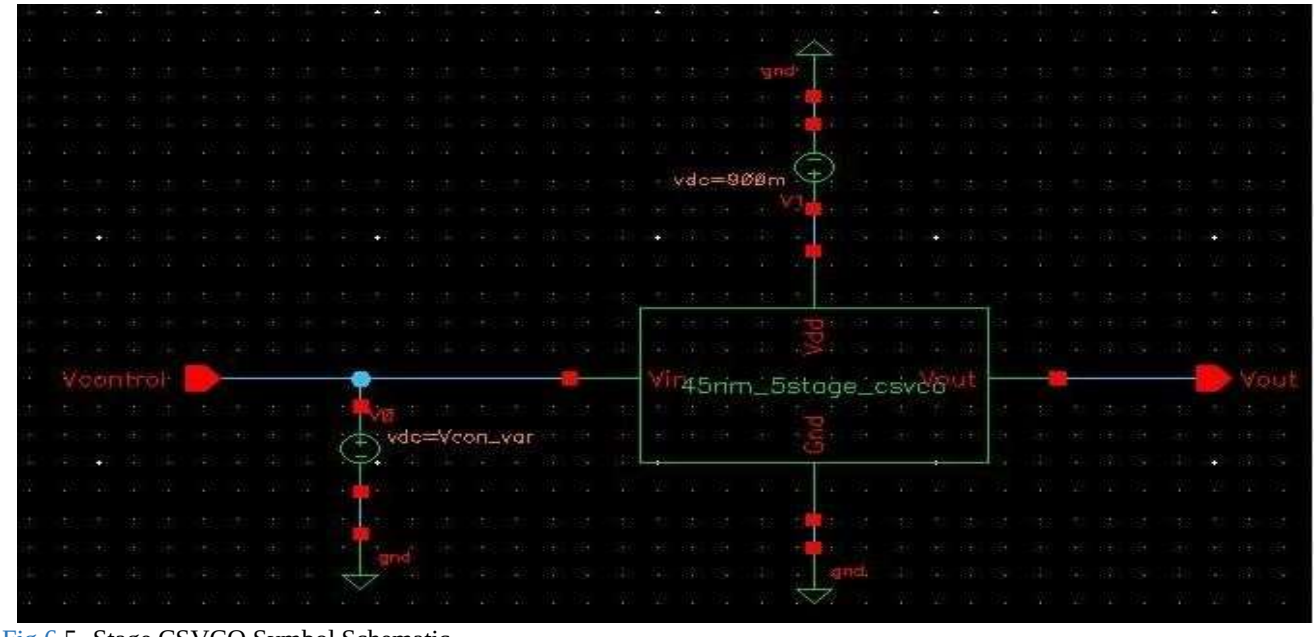


Fig.6 5- Stage CSVCO Symbol Schematic

The frequency of oscillation for N stage current starved voltage-controlled oscillator (CSVCO) is represented [26]

as:

$$fo = \frac{1}{T} = \frac{1}{2*N*td} \quad (2)$$

Where f_o is the frequency of oscillation of CSVCO. Total capacitance of CSVCO can be determined by the [27]-[30] following equation (3), equation (4), equation (5)

$$Ctot = Cout + Cin \quad (3)$$

$$Ctot = Cox(Ap + An) + \frac{3}{2}Cox(Ap + An) \quad (4)$$

$$Ctot = \frac{5}{2}Cox(Ap + An) \quad (5)$$

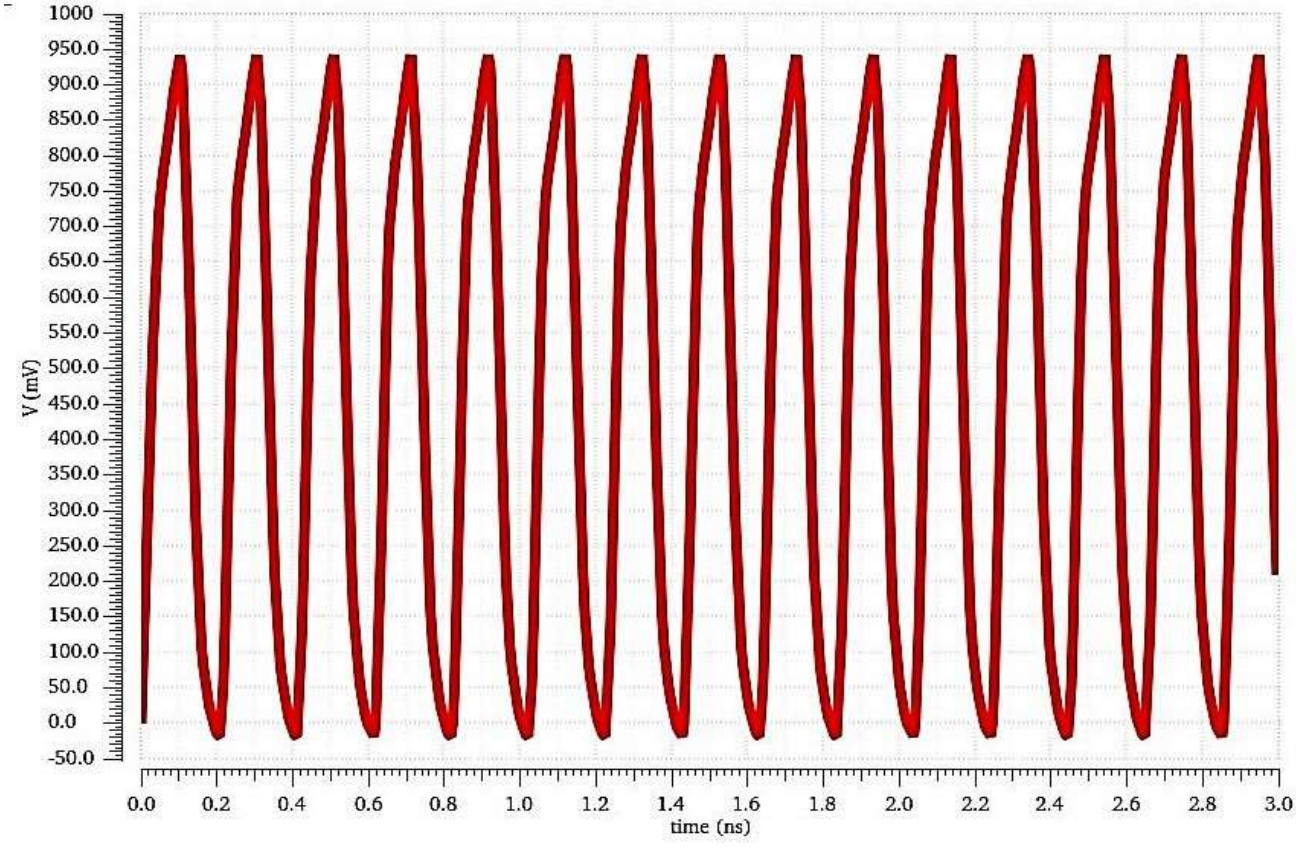
Where: $An = Wn * Ln$, $Ap = Wp * Lp$

Cox= oxide capacitance

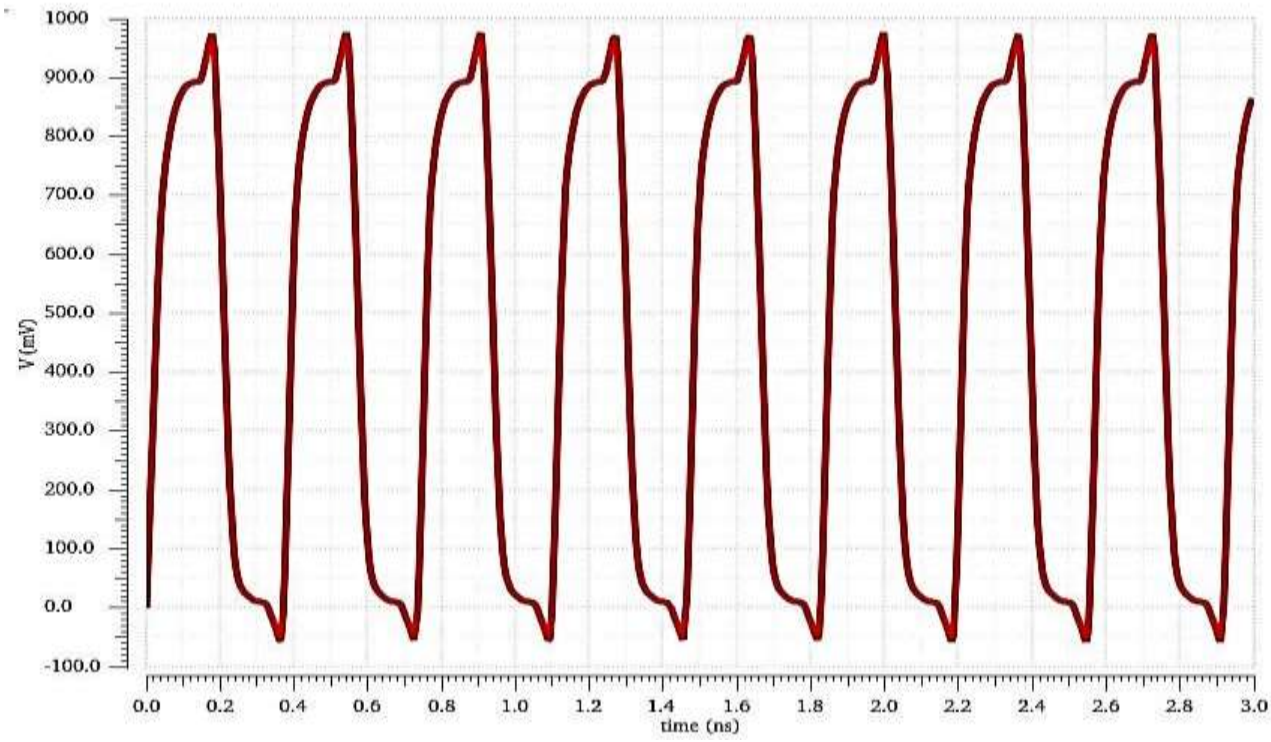
L_p, Ln are channel lengths and W_p, W_n are channel widths and A_p, A_n are cross sectional areas of the PMOS and NMOS transistors respectively [37-39].

4. Simulation and Result Discussion

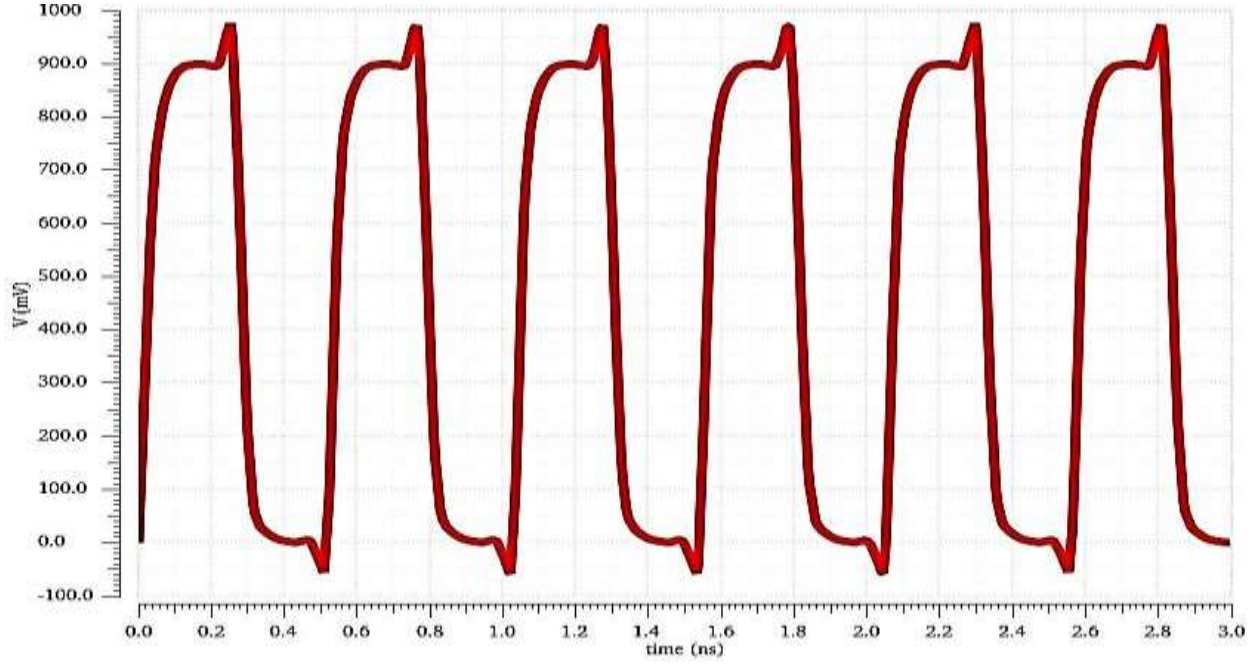
Cadence Virtuoso gpdk045nm technology has been used to build and simulate the proposed ring oscillator, 3-stage, 5-stage, and 7-stage CMOS current starved VCO (CSVCO). The standard schematic diagram of 3-stage, 5-stage, and 7-stage CMOS current starved VCO (CSVCO) is shown in Figure 3, Figure 4, and Figure 5, respectively. Figure 5 shows the schematic symbol of 5-stage CSVCO. Figure 7 shows the transient response of the CSVCO at 0.9 V of the CSVCO at an offset frequency of 2.419 GHz. Figure 8, Figure 9, Figure 10, and Figure 11 show the power consumption, phase noise, PSS analysis and V-control verses frequency graph of 3-stage, 5-stage, 7-stage CSVCO respectively. Table. 2 shows the V-control verses frequency Table of 3, 5, 7 stages CSVCO.



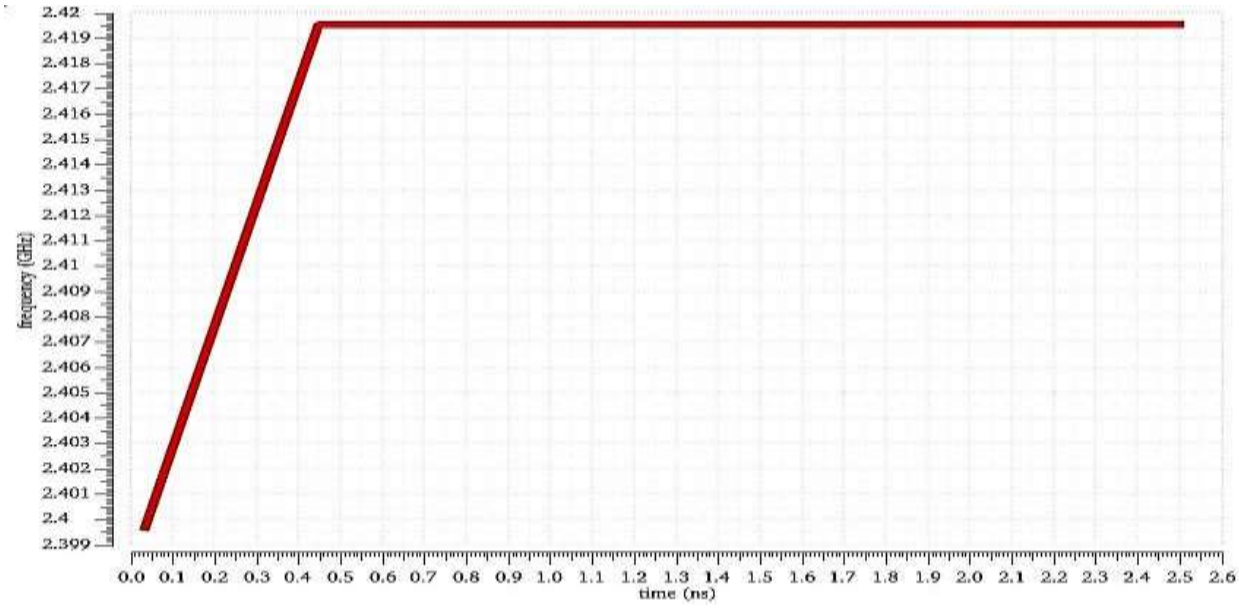
(a)


1000
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
V (mV)
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0
time (ns)

(b)

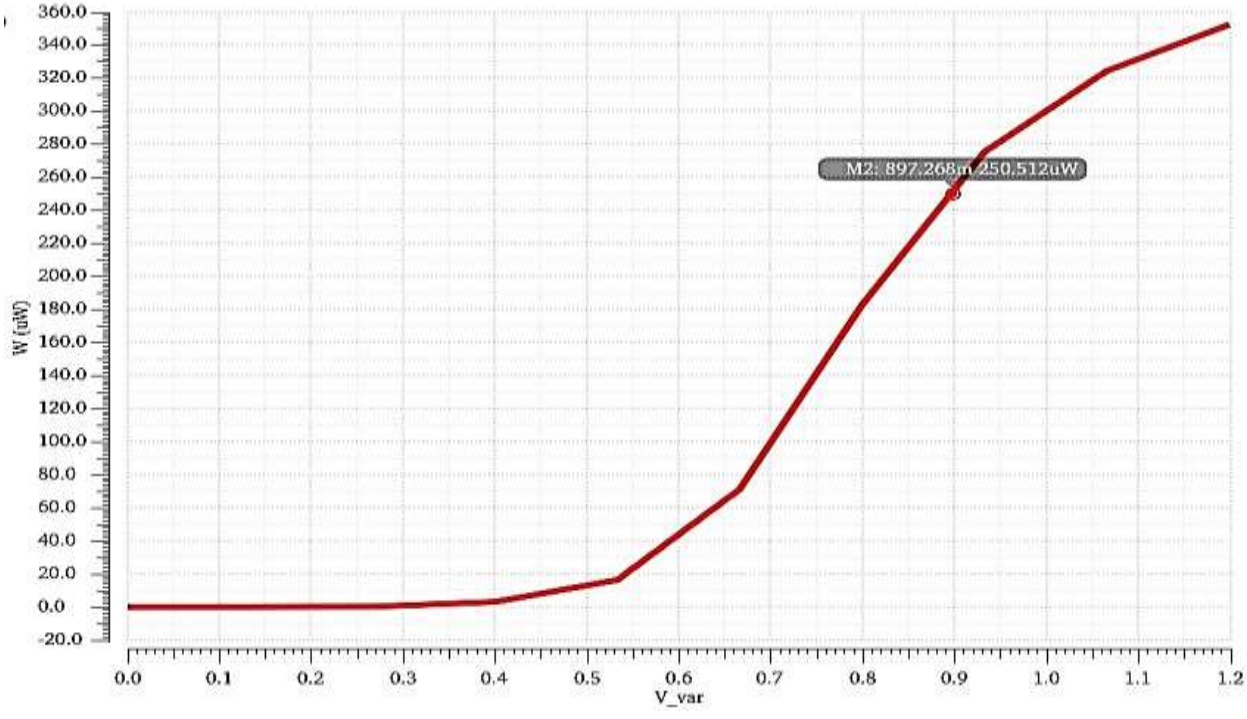

1000
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
V (mV)
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0
time (ns)

(c)

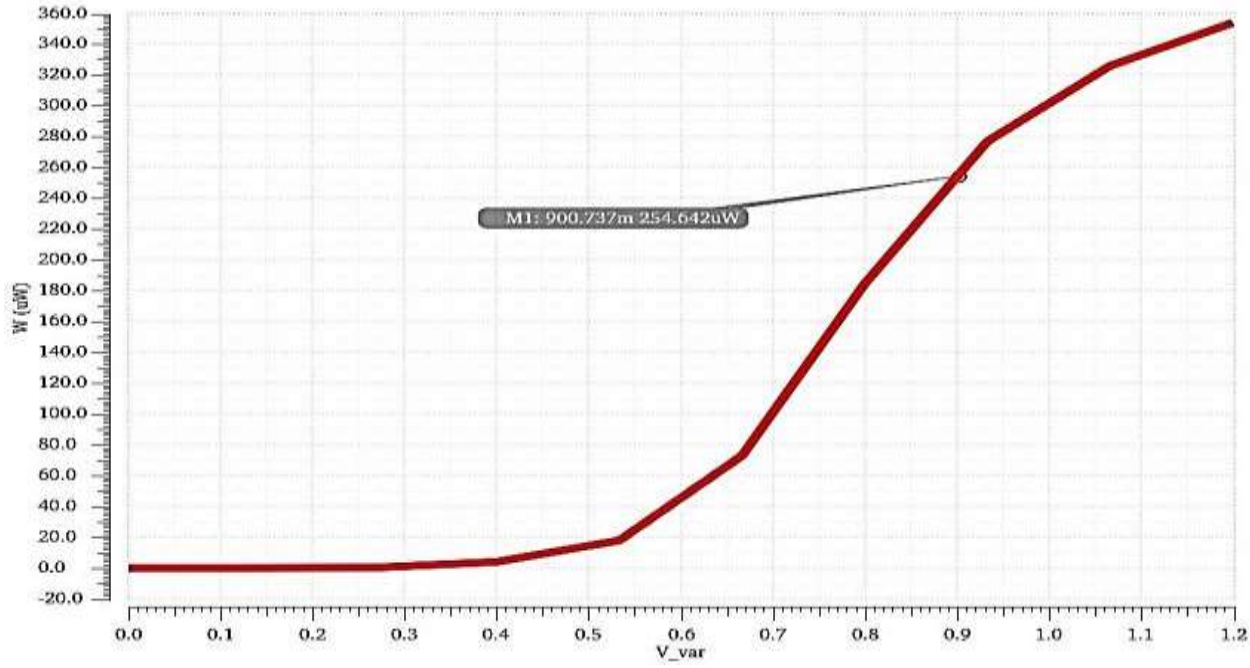


(d)

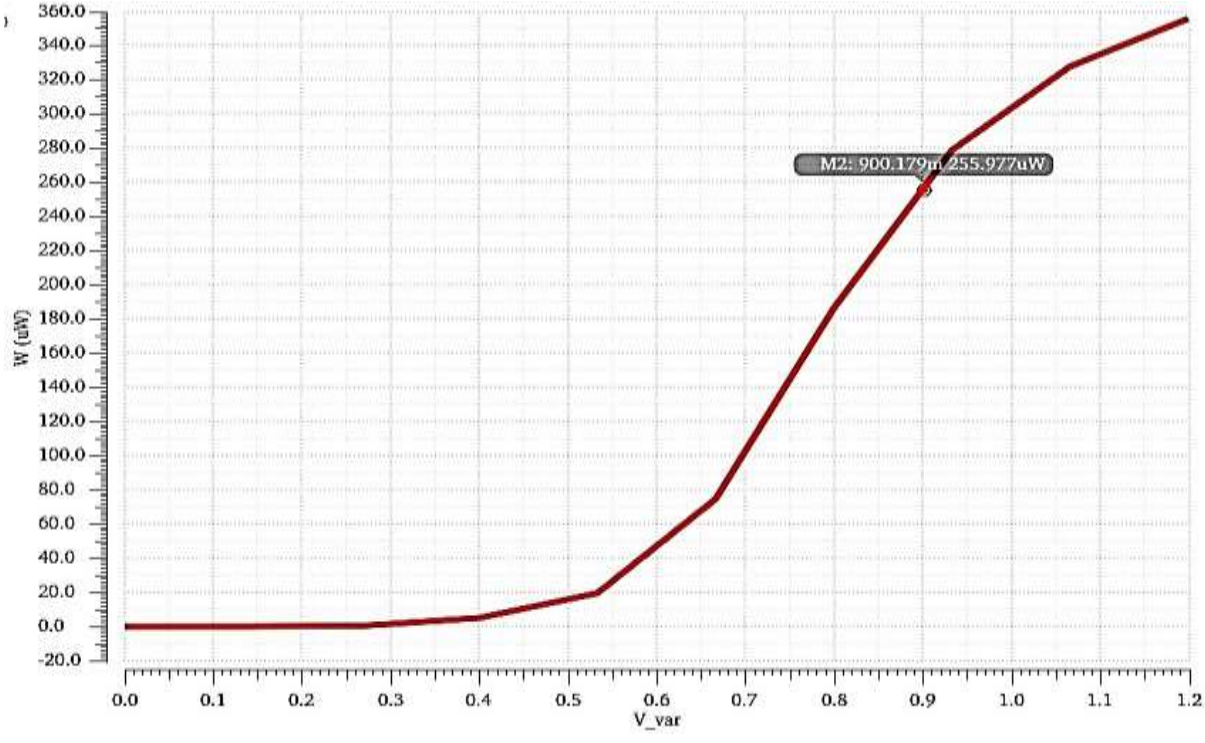
Fig.7 Transient response of (a) 3-stage CSVCO, (b) 5-stage CSVCO, (c) 7-stage CSVCO, (d) Center frequency



(a)

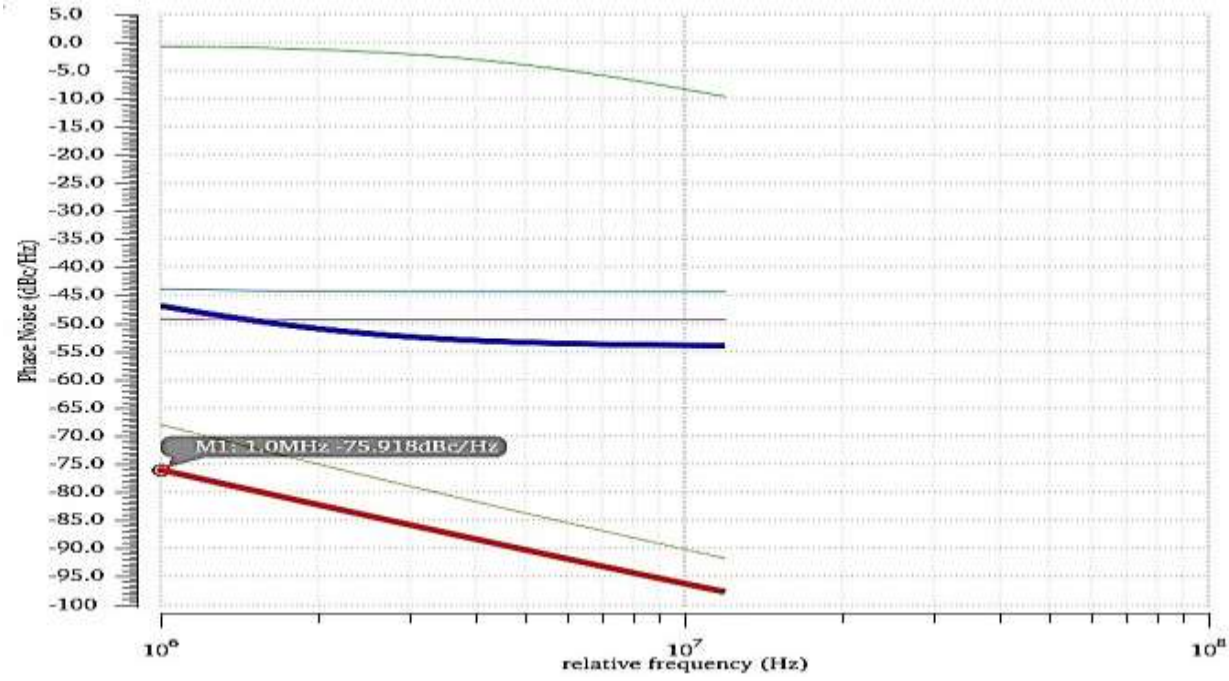


(b)

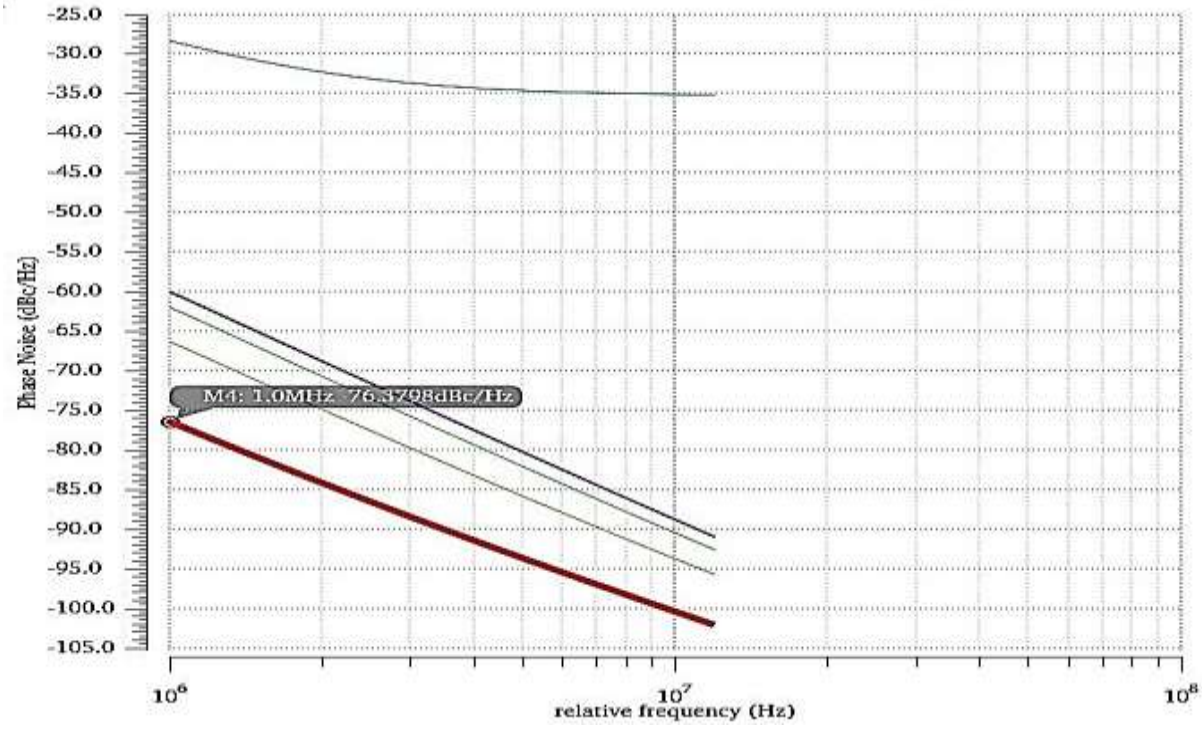


(c)

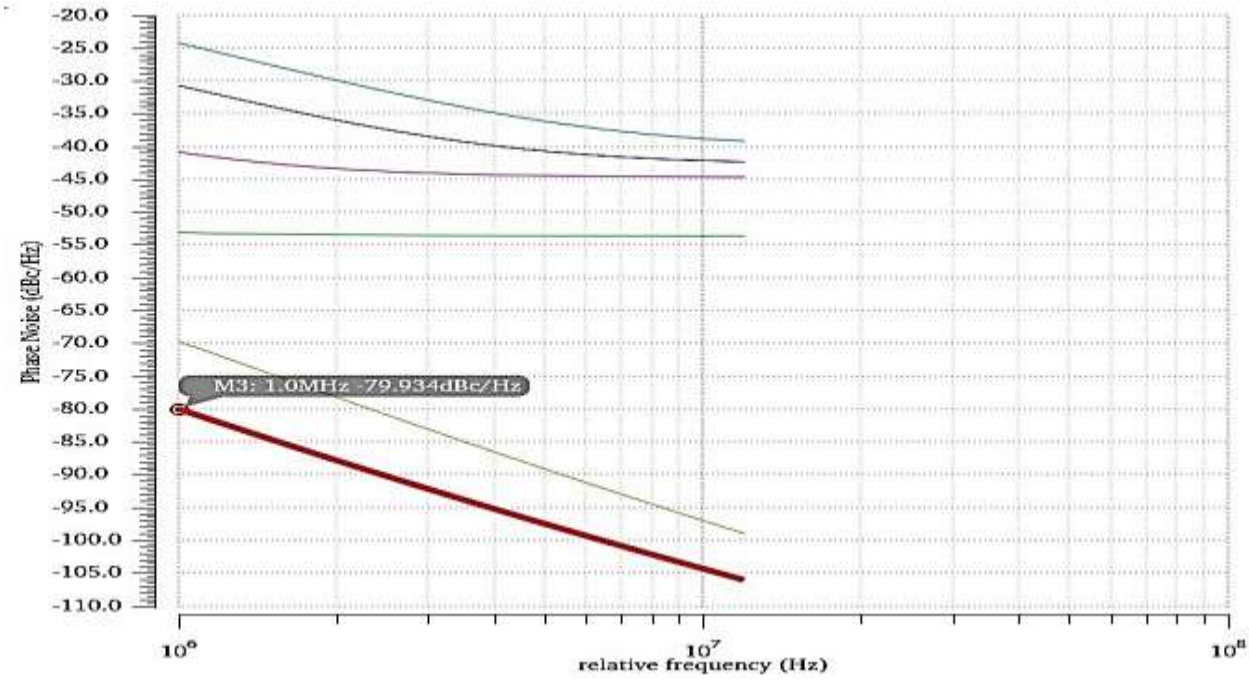
Fig.8 Power Consumption (a) 3-stage CSVCO, (b) 5-stage, (c) 7-stage CSVCO


5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
-45.0
-50.0
-55.0
-60.0
-65.0
-70.0
-75.0
-80.0
-85.0
-90.0
-95.0
-100
Phase Noise (dBc/Hz)
M1: 1.0MHz -75.918dBc/Hz
10^6
10^7
10^8
relative frequency (Hz)

(a)

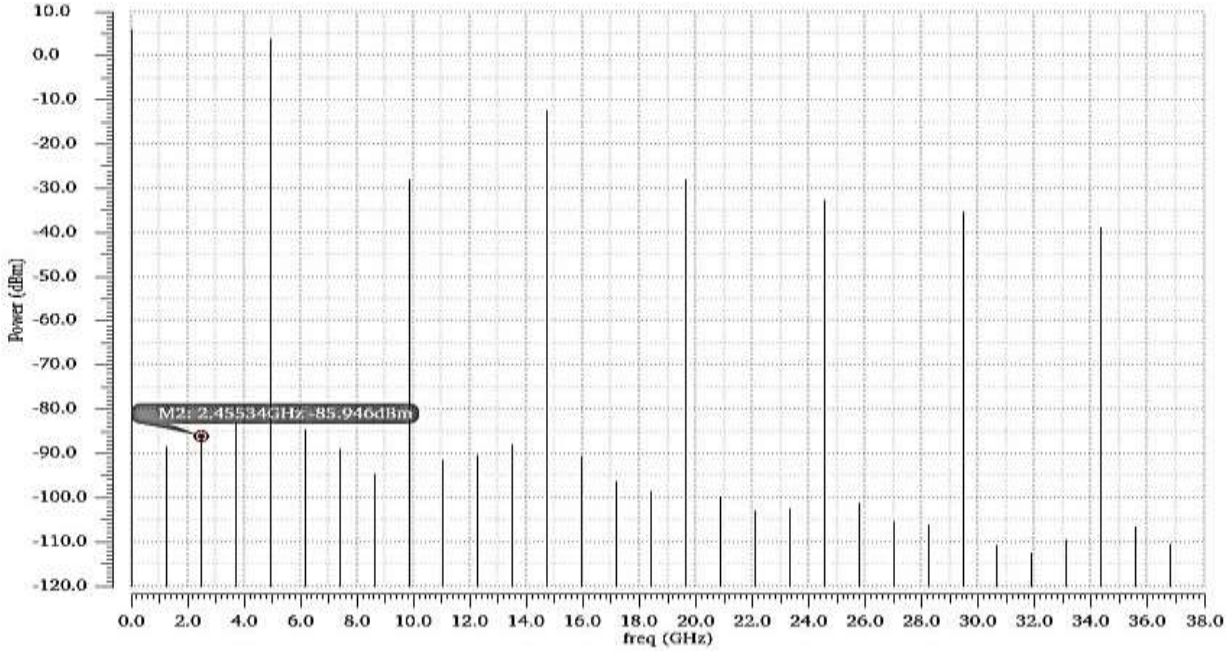

-25.0
-30.0
-35.0
-40.0
-45.0
-50.0
-55.0
-60.0
-65.0
-70.0
-75.0
-80.0
-85.0
-90.0
-95.0
-100.0
-105.0
Phase Noise (dBc/Hz)
M1: 1.0MHz -76.3798dBc/Hz
10^6
10^7
10^8
relative frequency (Hz)

(b)

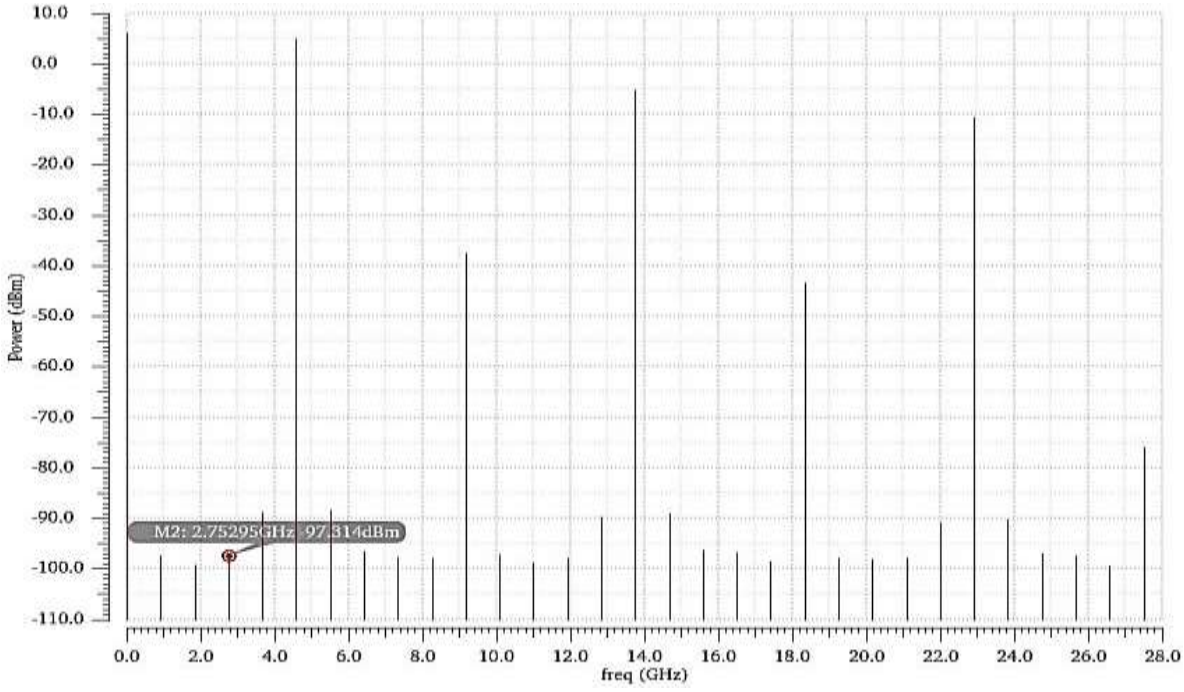


(c)

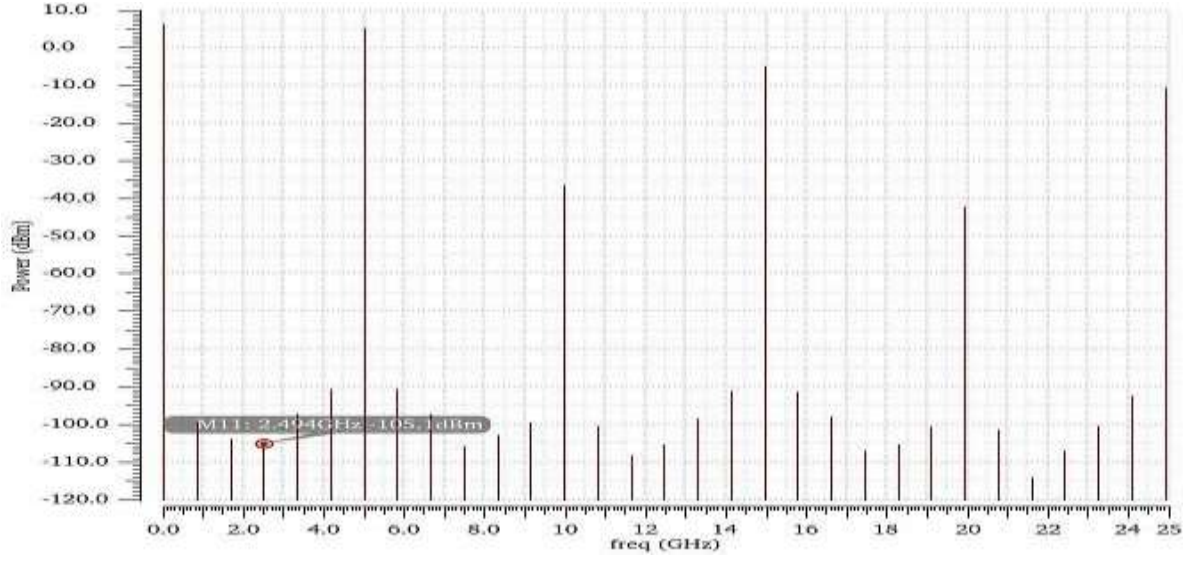
Fig.9 Phase noise (a) 3-stage CSVCO, (b) 5-stage CSVCO, (c) 7-stage CSVCO



(a)



(b)



(c)

Fig.10 Periodic steady state analysis (a) 3-stage CSVCO, (b) 5-stage CSVCO, (c) 7-stage CSVCO

Vcontrol (V)	3-Stage CSVCO	5-Stage CSVCO	7-Stage CSVCO
0.4	0.53	0.43	0.35
0.55	2.68	1.64	1.02
0.65	7.37	3.98	3.01
0.76	9.86	5.5	4.09
0.98	10.6	6.26	4.41
1.2	11.03	6.43	4.59

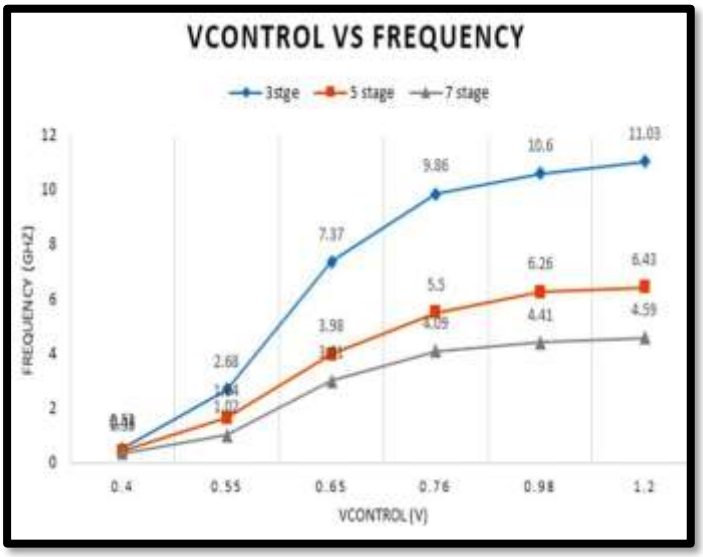


Fig.11 V-control verses Frequency Graph of 3-stage, 5-stage, 7-stage CSVCO

Table. 3 Comparative performance of CSVCO

Parameter	Technology (nm)	Voltage Supply (V)	Centre Frequency (GHz)	Power Consumption (mW)	Tuning Range (GHz)	Stages
[2]	90	1.1	2.0	0.765	"-"	13
[7]	28	1.0	2.0	0.370	0.025 to 0.200	5
[15]	500	5.0	0.025	0.817	0.001 to 0.026	9
[26]	90	1.0	6.22	0.368	4.22 to 6.22	3
[17]	90	1.8	0.015	2.150	0.007 to 0.016	7
[18]	180	1.8	2.138	3.140	0.109 to 2.148	5
[23]	45	1.0	3.22	0.100	1.5 to 3.22	5
	45	**0.9**	**2.4**	**0.250**	**0.534 to 11.036**	**3**
This work	**45**	**0.9**	**2.4**	**0.254**	**0.433 to 6.43**	**5**
	45	**0.9**	**2.4**	**0.256**	**0.353 to 4.59**	**7**

5. CONCLUSION

A low Power current starved ring VCO is developed using Cadence virtuoso gpdk045nm CMOS technology to serve broad band applications such as ISM, GSM, 900MHz cellular, RFID, SCADA, wireless security cameras, wireless video transmitters, wireless security systems, PCS, and Bluetooth. The current starved inverter delay cell structure and current mirror are optimized for the VCO's frequency tuning range, which is increased while keeping a low amount of phase noise [40]. The frequency tuning ranges of the proposed 3-stage, 5-stage, and 7-stage CSVCOs are 534.25 MHz to 11.036 GHz, 433.52 MHz to 6.43 GHz, and 353.18 MHz to 4.59 GHz, respectively. Phase noise of the 3-stage, 5-stage, and 7-stage CSVCOs at 2.419 GHz was measured at 1 MHz offset to be -75.91 dBC/Hz, -76.38 dBC/Hz, and -79.934 dBC/Hz, respectively. At a 0.9 V supply, it was discovered that the power consumption of a 3-stage, 5-stage, and 7-stage CSVCO was 250.512 µW, 254.642 µW, and 255.977 µW, respectively. In comparison to most designs performed using various CMOS technologies, the suggested VCO achieves wide tuning range and low power consumption, as demonstrated in Table 3. This study investigates the performance of multiple CS-VCO inverter stages of various sorts. According to the investigation, a 3-stage VCO uses less power than a 5- or 7-stage VCO and has poor phase noise performance than a 7-stage current-starved VCO. This performance analysis suggests using a 3-stage CS-VCO when power dissipation is the primary issue, but a 7-stage current starved VCO is used when better phase noise performance is required. VCO's higher oscillation frequency range makes it suitable for usage in ISM, Bluetooth, and GSM applications [41-45].

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AUTHORS

Nikhat Anjum received her bachelor's degree in Electronics and Communication Engineering from Institution of Engineers India (IEI), Kolkata, India, in 2011 and master's in technology in Electronics and Communication Engineering from Synergy Institute of Engineering and Technology, Dhenkanal, Odisha, in the year 2016. She is currently working towards a PhD degree in Electronics and Communication Engineering at Birla Institute of Technology, Mesra, Ranchi. Her research interests are microelectronics, low power very large-scale integration design, application-specific integrated circuit design, embedded system design.

E-mail: phdec10002.22@bitmesra.ac.in

https://orcid.org/0009-0009-3298-5805

Vimal Kumar Singh Yadav (Member, IEEE) received the BTech (Hons.) degree in electronics and communication engineering from Uttar Pradesh Technical University, India, in 2011, the MTech. degree from Tezpur University, Assam, India, in 2014, and the PhD degree from the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, Assam, in 2020. He has worked with the Centre for Nanotechnology, IIT Guwahati, as a Senior Research Fellow, for two years. He has worked as an Assistant Professor with the Department of Electronics and Communication Engineering, Birla Institute of Technology Mesra, Ranchi, Jharkhand, since September 2021 to April 2023. He is currently working as an Assistant Professor with the Department of Electronics and Communication Engineering, Motilal Nehru Institute of Technology Allahabad, Prayagraj. His research experience lies in the field of printed nanoelectronics, sensors, device fabrication, modelling, and simulation, nanobiotechnology, and magnetic devices.

E-mail: vksyadav@mnnit.ac.in

https://orcid.org/0000-0002-8987-9570

Vijay Nath received his BSc degree in physics from DDU University Gorakhpur, India in 1998 and PG Diploma in computer networking from MMM University of Technology Gorakhpur, India in 1999 and MSc degree in electronics from DDU University Gorakhpur, India in 2001 and PhD degree in electronics from Dr. Ram Manohar Lohiya Avadh University Ayodhya, India in 2008. His areas of interest are low power very large-scale integration design, application-specific integrated circuit design, embedded system design, internet of things, artificial intelligence & machine learning, and computational intelligence.

Corresponding Author

E-mail: vijaynath@bitmesra.ac.in

https://orcid.org/0000-0002-2601-1627