ISSN: 2584-0495 Vol. 1, Issue 2, pp.57- 63

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

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Cite as: Aprajita Bera, & Sudhakar S.Mande. (2023). Design and Optimization of Power Distribution Network (PDN) for improved Power Integrity(PI) performance using Plackett-Burman Design of Experiment (PB-DoE) Methodology. International Journal of Microsystems and IoT, 1(2), 57-63. https://doi.org/10.5281/zenodo.8275299

Published online:24 July 2023.

DOI: https://doi.org/10.5281/zenodo.8275299

International Journal of Microsystems and IoT
Vol. 1, Issue 2, pp. 57-63; DOI: https://doi.org/10.5281/zenodo.8275299

Design and Optimization of Power Distribution Network (PDN) for improved Power Integrity (PI) performance using Plackett-Burman Design of Experiment (PB-DoE) Methodology

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ABSTRACT

This paper discusses a novel methodology for optimization of design parameters for power integrity analysis. In the proposed methodology, Plackett-Burman Design of Experiment (PB-DoE) is utilized to determine the impact of design parameters on the response parameters. The design parameters are optimized to improve the dc voltage drop and dc current density. The impedance profile is compared for nominal and optimized design from 100MHz to 200MHz the obtained results are validated for thermal and noise performances. With this methodology, about 33% reduction is obtained in the dc drop voltage and dc current density with about 1% to 5% improvement in thermal performance.

KEYWORDS

HyperLynx; Optimization; PI simulation; Power Integrity; Power Distribution Network; Plackett –Burman DoE

1. INTRODUCTION

Advancements in the VLSI technology have led to the miniaturisation of devices and lowering of operating voltage and current. This has resulted in power integrity analysis as an inevitable part of a successful design. To study the delivery of clean power throughout the network, the analysis of power distribution network has become crucial to limit the voltage ripples and also for reduction in voltage disturbance arising due to switching [1]-[2]. Development of Power Integrity analysis methodology is necessary to solve the challenges of high-speed design by optimising the design parameters [3]-[5]. In [6] different aspects of PDN analysis are described for AC Power Integrity and DC Power Integrity analysis using Mentor Graphics HyperLynx PI simulation tool.

In DC analysis, it is essential to ensure that maximum voltage drop does not exceed the tolerance of operating voltage supplied to the load, which can result in malfunction of the system. The maximum DC drop voltage obtained for 1.2 V power rail is 6.8 mV, which is within ±2.5% tolerance. AC analysis examines the frequency response of characteristics impedance of the power distribution network [7]-[8].

The impact of various design parameters in the DC and AC power integrity analysis is discussed in [9]-[12]. Analysis and optimisation of the input design factors affects the response parameters and hence helps in improving the design of power distribution network. Design of Experiment method (DOE) is a well-known statistical technique used to quantify the effect of various input factors on the output response of a system with minimum number of experimental/Simulation runs. The Plackett–Burman DOE (PB-DOE) method has been widely used to investigate the effect of variations in process parameters on device and circuit performance [13-15].In this paper, pre-layout dc and ac analysis is discussed, and the values of the input parameters are optimised after studying their effects on the response parameters. In Section 2, the methodology for power integrity analysis is discussed. In Section 3, optimisation of the input design factors is discussed using PB-DoE. The obtained optimised design is validated using thermal and noise analysis and is shown in section 4.

2. METHODOLOGY FOR POWER INTEGRITY ANALYSIS

In this paper the power integrity DC and AC Analysis of 6 layers stack up PCB is discussed. The simulation is done with Mentor Graphics HyperLynx PI Simulation tool and the optimised parameters are obtained using Plackett- Burman Design of Experiment method.

Power Integrity analysis has two aspects DC analysis, also known as IR, drop analysis and AC analysis, which is dynamic in nature and is also referred to as AC ripple voltage analysis. In this paper two test design cases are considered. The schematics and the board sim layout of the both the designs are used with editor tool for PI DC analysis and the performance parameters are obtained.The parameters are modified, and the impedance profile is compared for nominal values and optimised values of the design parameters.

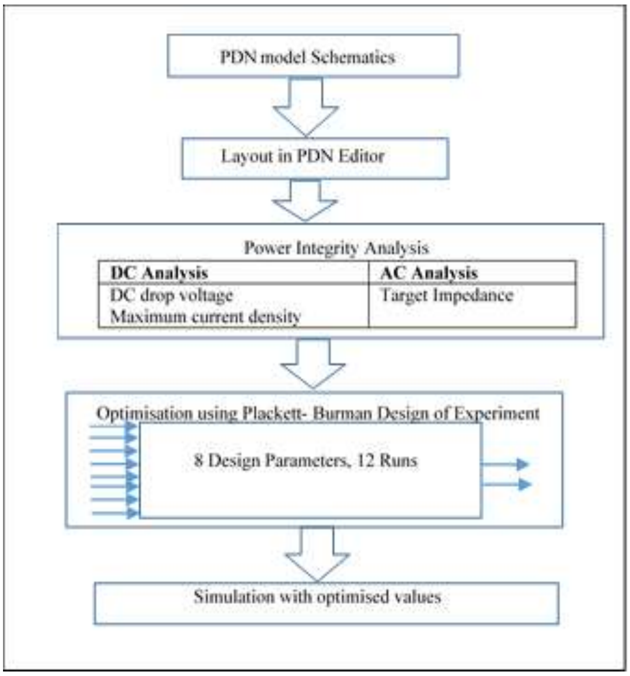

Fig.1 Design flow for PI analysis

Pre route DC analysis is the static PDN analysis, where the voltage requirement, tolerance and maximum current for corresponding power rail is derived from the specific data sheet. The design parameters and their nominal values are listed in Table 1

Table. 1 Models and specifications

Model	Specifications
PIC1	0.5A, 1000000Ohm (each)
PIC2	0.25A, 1000000Ohm (each)
C1	C=2.2uF, ESL=2400pH, ESR=0.5mOhm
	C=47uF, ESL=255pH, ESR=0.5mOhm

The VRM model is chosen with 1.2V power rail (Ro=1mΩ, Lout=30000nH, Rflat=10Ω, L slew=10μH). Two arrays of IC power pins are mounted on the Top layer with DC sink model assigned to them. Two arrays of decoupling capacitors are added on the top layer and are represented as the series connection of ESR, ESL and C . Two arrays of Vias are attached to the top layer and connect to inner signal 1 layer and bottom layer respectively. Table 1 shows the models used for the design and their specifications. Table 2 shows the symbol of the parameters.

Table. 2 Parameter values and symbols

Symbol	Parameter
P1	Number of power IC ,0.5A
P2	Area for array PIC1
P3	Number of power IC ,0.25A
P4	Area for array PIC2
P5	Number of decoupling capacitors C1
P6	Area for array for decoupling capacitors C1
P7	Number of decoupling capacitors C2
P8	Area for array for decoupling capacitors C2

The main objective of AC power integrity analysis is to minimise the impedance of the power distribution network Zpdn over a band of chosen frequency. The frequency dependent impedance profile should be below target impedance Ztarget to avoid voltage noises during the switching action and hence to provide clean power supply throughout the network. Target Impedance is the ratio of allowable voltage ripple to the maximum transient current. The value of target impedance can be calculated as

$$Ztarget = \frac{\text{VDD}*\text{Ripple }\%}{Itransient} \quad (1)$$

Where, VDD is the supply voltage of interest, Ripple % is the AC ripple margin and Itransient is the maximum current transient throughout the load.

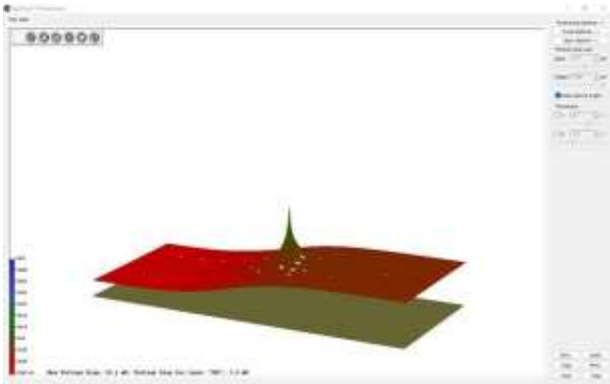

Fig.2 DC voltage drop for Design 1 with nominal values10.1 mV

The target impedance for this design is calculated to be 330mΩ. Plackett- Burman design of experiment method is used for further optimisation of the dc drop voltage value with evaluation of parameters.

3. OPTIMIZATION USING PB DOE

The Plackett-Burman DoE methodology is a unique technique to statically evaluate the effect of design parameters on the performance of the circuit with a number of simulations runs. Thus, identifying the significant parameters at the starting of design cycle. The orthogonal matrix is generated with design parameters that can be both qualitatively and quantitatively defined with '+' and '-' sign.

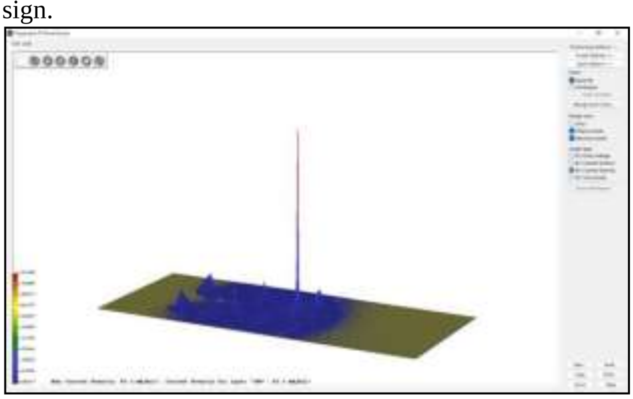

Fig.3 Current density for Design 1 with nominal values 83.3 m A/mil2

For quantitative design parameter, '+' or '-' represents a ±30% deviation from the nominal design parameters respectively. Design parameters which are qualitative are considered 'high' and 'low' for '+' or '-'. In this paper, the impact of design parameters (P1-P8) deviation on the performance parameters EA and EB is observed over 12 simulation runs (R1-R12). The PB-DoE matrix as shown in table 3 for 8-parameter design [13]-[16]. The number of response parameters can vary as per the experiment

Table. 3 Generation of Orthogonal matrices for 8 parameters and 12 runs

R/P	P1	P2	P3	P4	P5	P6	P7	P8	EA	EB
R1	+	-	+	-	-	-	+	+	EA1	EB1
R2	+	+	-	+	-	-	-	+	EA2	EB2
R3	-	+	+	-	+	-	-	-	EA3	EB3
R4	+	-	+	+	-	+	-	-	EA4	EB4
R5	+	+	-	+	+	-	+	-	EA5	EB5
R6	+	+	+	-	+	+	-	+	EA6	EB6
R7	-	+	+	+	-	+	+	-	EA7	EB7
R8	-	-	+	+	+	-	+	+	EA8	EB8
R9	-	-	-	+	+	+	-	+	EA9	EB9
R10	+	-	-	-	+	+	+	-	EA10	EB10
R11	-	+	-	-	-	+	+	+	EA11	EB11
R12	-	-	-	-	-	-	-	-	EA12	EB12

The values of each parameter with subsequent runs and the result of each run is recorded as E1-E12 for EA (max voltage drop measured in mV) and EB (maximum current density measured in mA/mil2) .The nominal and the optimised values of the design parameters are shown in the table 4. The optimised value of the design parameters is selected depending on their desirable effect on the response parameters. The optimised values of the design parameters are used to draw the impedance profile for a frequency band of 100 MHz to 200 MHz. The same methodology is used for another design with LVCMOS25_F_24 driver. The values for the design parameters (P1-P8) and the performance parameters EA and EB for both Design 1 and Design 2 are shown in Table **4.** The value of the performance parameters has improved for both the optimised designs.

Table. 4 Nominal and optimized parameters for Design1 and Design 2

Parameters	Design 1 Nominal	Design1 Optimised	Design 2 Nominal	Design2 Optimised
P1(N1PIC1)	6	4	6	4
P2(S1PIC1) ($inch^2$)	5.63	5.06	0.3	0.309
P3(N2PIC2)	6	4	4	5
P4(S2PIC2) ($inch^2$)	1.71	1.88	0.32	0.33
P5(N3C1)	32	36	8	6
P6(S3C1) ($inch^2$)	13.37	14.71	0.48	5
P7(N4C2)	12	10	12	14
P8(S4C2) ($inch^2$)	5.95	6.55	0.29	0.28
EA (mV)	10.1	6.8	7.7	5.2
EB (mA/mil^2)	83.3	55.6	58.1	40.2

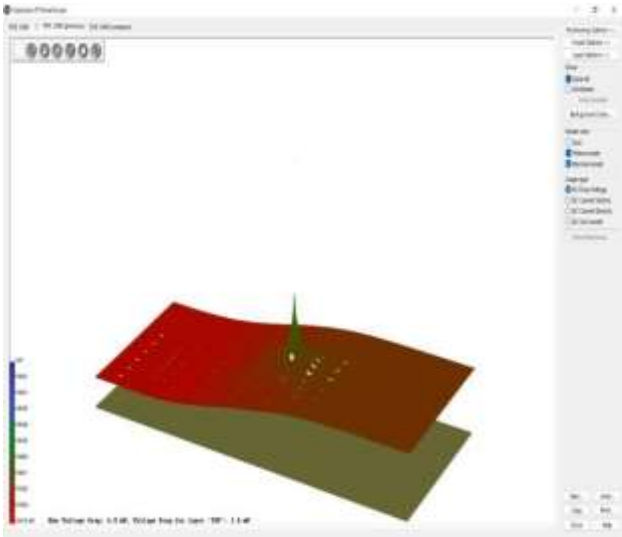

Fig.4 DC voltage drop for Design 1 with optimized values 6.8 mV

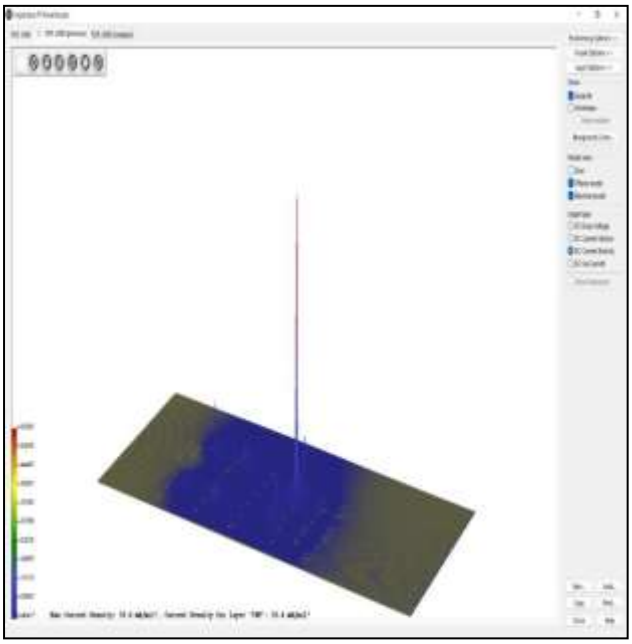

Fig.5 Current density for Design 1 with optimized values 55.6m A/mil^2

Impedance profile drawn with the optimised design parameters is compared with the impedance profile of nominal parameters and is shown in figure 6 and figure 7.For both the designs , with nominal values the impedance profile exceeds the target impedance line .With optimization of the design parameters the impedance profile of the power distribution network lies below the target impedance and is observed in frequency range between 100 MHz to 200MHz.

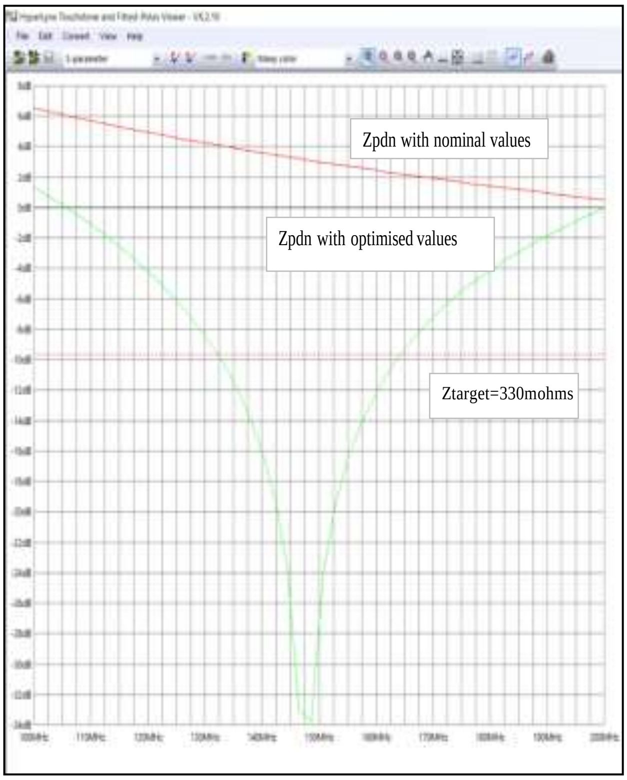

Fig.6 Impedance profile for nominal values (red) and optimized values (green) for design 1

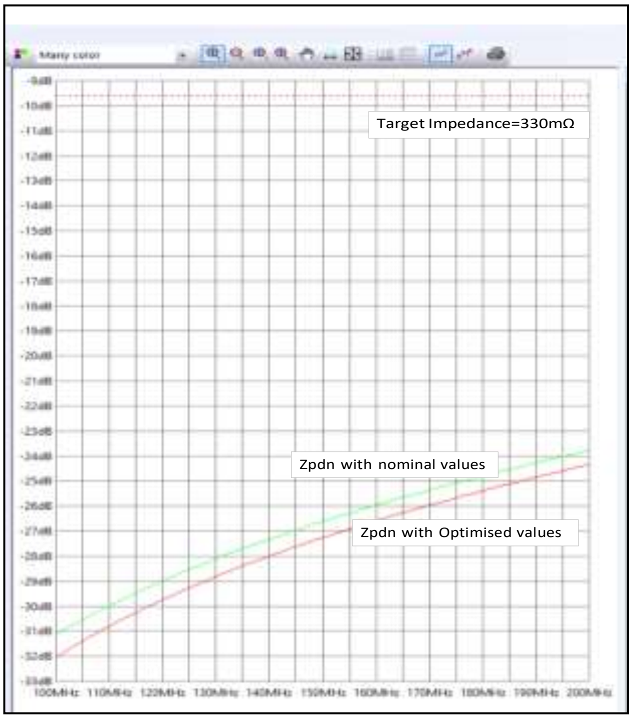

Fig.7 Impedance profile for nominal values (red) and optimized values (green) for design 2

Table 4 shows about 33% improvement in power integrity performance of the optimized design. This novel optimization methodology derives the holistic effect of the variations of all the significant design parameters towards the improved power integrity performance. The previously used optimization techniques lacked to analyze the complete effect of the variation in input design parameters.

Table 5 shows the pre-existing optimization techniques and a comparison with the current technique.

Table. 5 Comparison of improvement in performance with earlier optimization techniques

Parameter	Effects	Improvement with earlier techniques	Improvement with current technique
Via current, plane dimension, decoupling capacitors, Ztarget [6]	Pre route AC and DC analysis	13.8% reduction in dc drop voltage	Reduction in DC drop voltage for both design 1(10.1 mV to 6.8 mV) and design 2(7.7 mV to 5.2 mV)
Hybrid Target Impedance [17]	Mitigates over design	30% reduction in voltage specification	Reduction max DC current density in design1 (83.3 mA/mil^2 to 55.6 mA/mil^2) and design2 (58.1mA/mil^2 to 40.2 mA/mil^2)
PDN impedance [18]	Voltage drop estimation by varying decoupling capacitor placement.	27.1% reduction in dc voltage drop	
Hybrid Target Impedance [19]	Decoupling capacitor optimization	35% reduction in voltage specification	Improvement in thermal performance for both designs (1% to 5%)
Decoupling capacitor [20]	Impedance profile is maintained below Ztarget	2% reduction in decoupling capacitor	Reduction in noise voltage in design1 (3%) and design2 (14.5%)

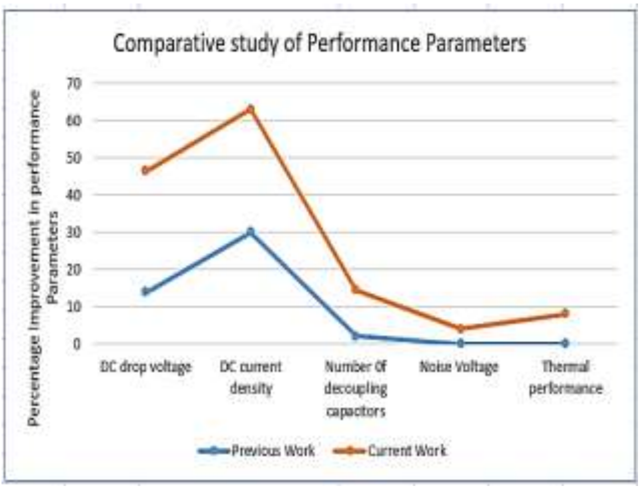

Fig.8 Comparative study of performance parameters on

optimization of Power Distribution Network

4. VALIDATION

The optimized designs obtained are validated by thermal analysis and measuring the noise voltage. This helps to identify any trade-offs occurring in the optimised design while giving better DC drop parameters and target impedance. DC drop and thermal analysis are co-related. Very high temperature of the board can further increase the dc drop voltage and high current density can increase the board temperature. Figure 8 and 9 shows that the optimised designs show better thermal analysis as well.

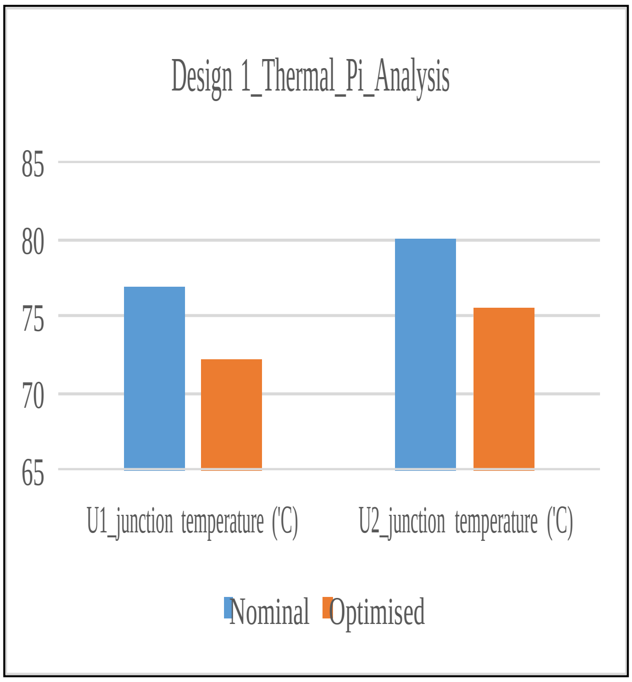

Fig.9 Junction temperature for power ICs for design 1

Power Integrity also shows the effect of non-ideal behaviour of the power plane. Noise voltage measures the signal via and power plane interaction and gives an accurate analysis of the net's performance [21-27]. In this case, noise voltage has reduced for both the optimised designs as shown in figures 11 to 14. Thus, both the designs give better values of thermal and noise performance.

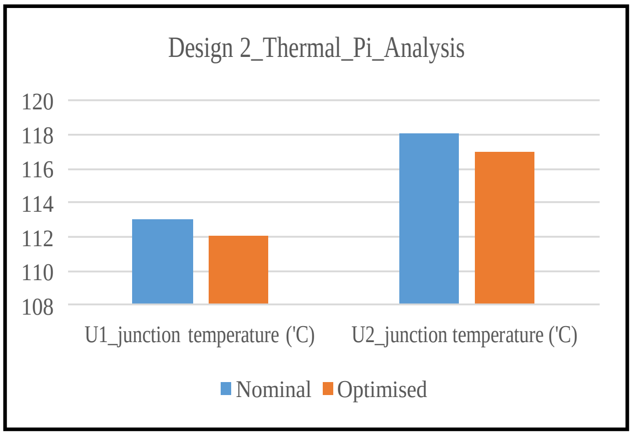

Fig.10 Junction temperature for power ICs for design 2

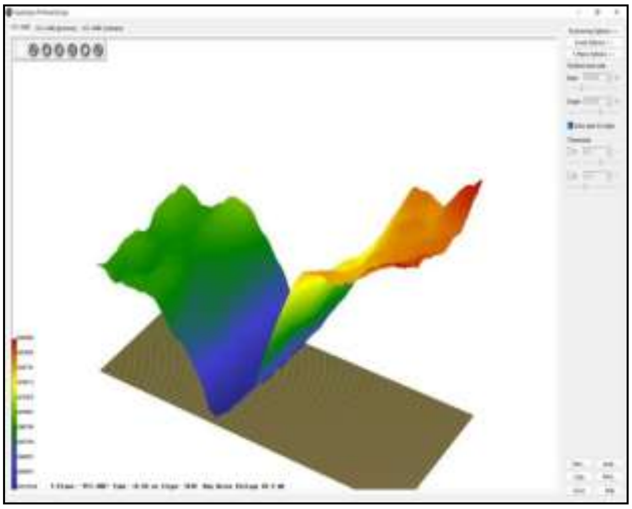

Fig.11 Noise voltage for Design1 with nominal values

86.9 m V

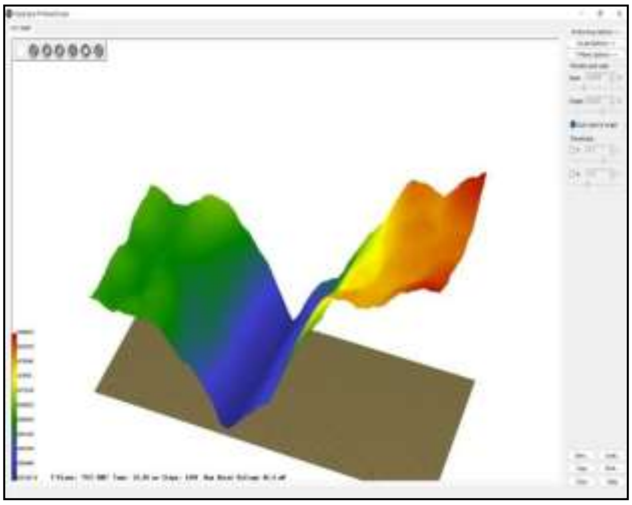

Fig.12 Noise voltage for Design1 with optimized values

86.6m V

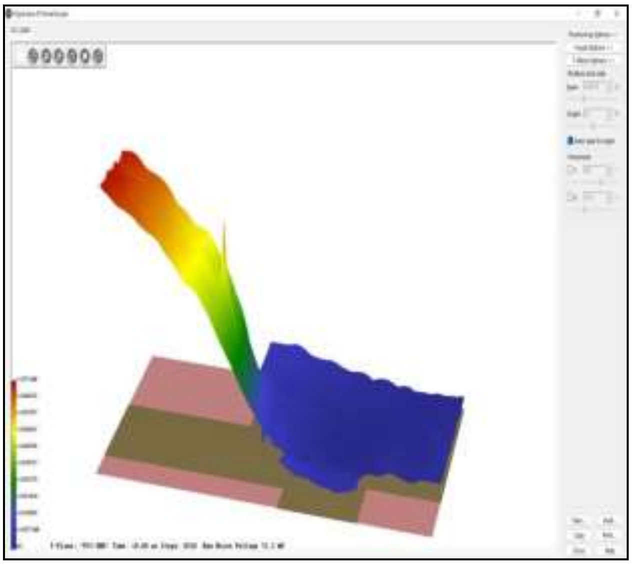

Fig.13. Noise voltage for Design 2 with nominal values 71.3 m V

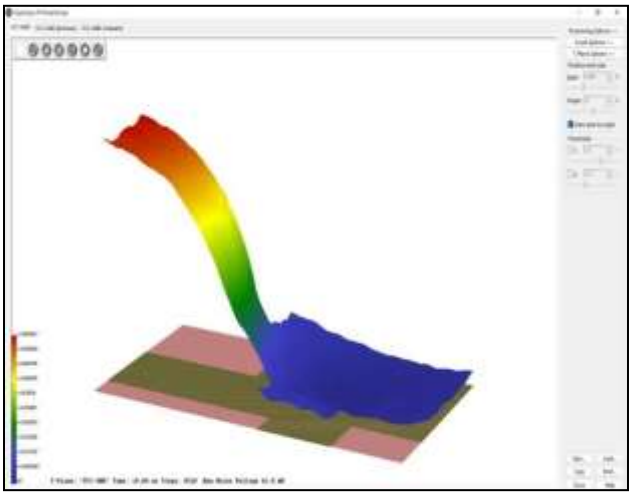

Fig.14. Noise voltage for Design 2 with optimized values 61V

5. CONCLUSION

In this paper the DC and AC power integrity analysis is discussed. The simulations are performed using Mentor Graphics HyperLynx PI tool. The optimization of the design is done by statistical method using Plackett-Burman design of experiments. This methodology improves the dc drop voltage, dc current density and the impedance profile. The dc drop voltage has reduced from 10.1 mV to 6.8 mV and dc current density have reduced from 83.3 mA/mil2 to 55.6 mA/mil2 for design 1. The dc drop voltage has reduced from 7.7 mV to 5.2 mV and dc current density have reduced from 58.1 mA/mil2 to 40.2 mA/mil2 for design 2. The PB-DoE methodology has shown 33% improvement in power integrity performance as compared to the conventional method. The optimised designs have shown better noise and thermal performance. This methodology can be further developed and tested for different driver models and different board shapes. The results obtained validates the suitability of PB-DoE for better power integrity performance.

ACKNOWLEDGEMENTS

The authors acknowledge Sardar Patel Institute of Technology, Mumbai, India for providing all the resources for this research.

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