ISSN: 2584-0495 Vol. 1, Issue 1, pp.26-34

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

An Ultra Low Power CMOS Sigma Delta ADC Modulator for System-On-Chip (SoC) Micro-Electromechanical Systems (MEMS) Sensors for Aerospace Applications

Jeet Tirkey, Sarvesh Dwivedi, Sanjay Kumar Surshetty, T. Snehitha Reddy, Manoj Kumar, Vijay Nath

Cite as: Jeet Tirkey, Sarvesh Dwivedi, Sanjay Kumar Surshetty, T. Snehitha Reddy, Manoj Kumar, & Vijay Nath. (2023). An Ultra Low Power CMOS Sigma Delta ADC Modulator for System-On-Chip (SoC) Micro-Electromechanical Systems (MEMS) Sensors for Aerospace Applications. International Journal of Microsystems and IoT, 1(1), 26–34. https://doi.org/10.5281/zenodo.8186894

Published online: 26 June 2023.

DOI: https://doi.org/10.5281/zenodo.8186894

International Journal of Microsystems and IoT
Vol. 1, Issue 1, pp.26-34; DOI: https://doi.org/10.5281/zenodo.8186894

An Ultra Low Power CMOS Sigma Delta ADC Modulator for System-On-Chip (SoC) Micro-Electromechanical Systems (MEMS) Sensors for Aerospace Applications

Jeet Tirkey[1], Sarvesh Dwivedi[1], Sanjay Kumar Surshetty[1],T. Snehitha Reddy[1], Manoj Kumar[2], and Vijay Nath[1]

[1]Birla Institute of Technology, Mesra, Ranchi, India
[2]Digital Image Forensics, The North cap University Gurugram , India

ABSTRACT

This paper presents the design and implementation of an ultra-low power CMOS sigma-delta analog-to-digital converter (ADC) modulator specifically tailored for System-on-Chip (SoC) micro-electromechanical systems (MEMS) sensors utilized in aerospace applications. The proposed ADC modulator aims to address the stringent power constraints while maintaining high-resolution and accuracy requirements for the acquisition of sensor data. The proposed ADC modulator leverages the sigma-delta modulation technique, known for its effectiveness in achieving high resolution with low-power consumption. The design focuses on minimizing power consumption by employing innovative circuit architectures, low-voltage supply, and reduced transistor sizes. This design incorporates the utilization of 180nm technology, resulting in an average power consumption of 54 µW when operated at a sampling frequency of 50 MHz It efficiently operates within a narrow power supply range of +1.3V to -1.3V.

KEYWORDS

Clocked comparator; CMOS; DAC;D flip flop; Integrator; Op-amp; Signal to Noise Ratio (SNR)

1. INTRODUCTION

The rapid progress of technology has facilitated the integration of an entire circuit system onto a single chip. To convert the analog signal received from the system-on-chip Micro-Electromechanical Systems (MEMS) sensor into the digital domain, an analog-to-digital converter (ADC) is required that is high-performance, minimally inaccurate, more effective, reliable, and resilient. Comparatively, data in the digital domain is significantly safer, more transferable, and easier to duplicate than in the analog domain. Among available ADC options, the Sigma Delta (ΣΔ) ADC stands out as the optimal choice due to its ability to achieve high precision, along with a good signal- to-noise ratio (SNR). The Sigma Delta (ΣΔ) ADC comprises two essential components: the digital filter and the sigma delta modulator. The digital filter prioritizes time resolution over amplitude, while the modulator component combines sampling at a rate equal to or higher than the Nyquist rate with negative feedback[1]. Furthermore, the sigma delta (ΣΔ) ADC demonstrates a remarkable tolerance for imperfections in analog circuits, enabling the implementation of high-density and sophisticated analog circuits using Sigma Delta (ΣΔ) technology.

Consequently, it becomes a top priority for system-on-chip (SoC) implementation. The block diagram for a sigma delta modulator is depicted in Figure 1. One crucial component of the sigma delta (ΣΔ) ADC modulator is the integrator, which has been purposefully designed. In the high-order sigma delta (ΣΔ) ADC modulator's forward path, multiple integrators are employed, ensuring excellent resolution but also making it susceptible to instability [1], [2]. While it is possible to cascade a single-order sigma delta (ΣΔ) ADC modulator to achieve precise gain, the order of the sigma delta (ΣΔ) ADC modulator is influencedby application-specific factors. By sampling the input signal at a high frequency, the sigma delta (ΣΔ) ADC modulator converts the analog signal into a digital pulse. However, if poor filtering is present, the resulting digital pulse becomes contaminated with unwanted noise, as evidenced in [3] and [4]. The choice of the modulator's sampling ratio and order at the modulator stage directly impacts the output's resolution. Since the analog input signal can now be directly sampled using an oversampling clock [6], [7], the previously contemplated need for ananti-aliasing filter is no longer necessary.

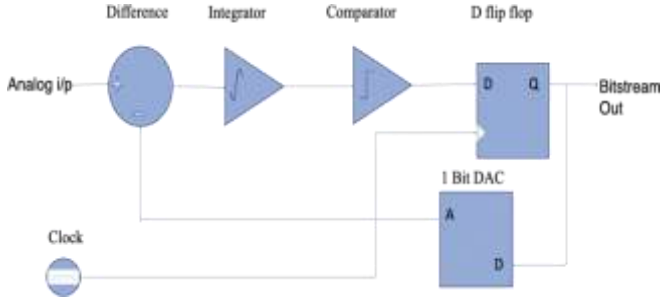


Fig. 1 Block diagram of Sigma Delta ADC

Therefore, in this research, we propose and validate an improved and precise ultra-low-power sigma delta (ΣΔ) ADC modulator. The remaining sections of the paper adhere to the following structure. Section II provides a detailed explanation of the suggested circuit configuration, accompanied by a comprehensive illustration of each individual component. The findings and subsequent discussion are the primary focus of Section III, while the work is ultimately concluded in Section IV. Figure 1 showcases the sigma delta (ΣΔ) ADC modulator, consisting of various components including a difference amplifier, an integrator, a comparator, a D flip flop, and a DAC.Prior to being converted into a pulse train at the

output, the input analog signal has gone through numerous steps such as oversampling, quantization, and noise shaping. Modern technology conserves a critical amount of space through both the analogue to digital (ADC) and digital to analog (DAC) conversion procedures [8], [9].

2. PROPOSED CIRCUIT CONFIGURATION

2.1 Operational Amplifier

An operational amplifier (op-amp) is an electronic amplifier extensively utilized in a diverse range of analog circuits. It functions as a voltage amplifier with high gain, capable of amplifying the discrepancy between two input signals to generate an output signal. In order to ensure stability of the system, the implementation of the Miller compensation technique is incorporated into the op-amp circuit. Op-amps are engineered with a multitude of characteristics that contribute to their versatility and effectiveness in various applications. These characteristics encompass high gain, high input impedance, low output impedance, a high common-mode rejection ratio (CMRR), and low input offset voltage and current[10].

The open-loop gain of an op-amp, which refers to its gain without any feedback, is a crucial characteristic. It is typically remarkably high, often reaching tens of thousands or even millions. However, the open-loop gain of an op-amp is prone to instability and oscillations over a wide range of frequencies or temperatures[11]. To overcome this limitation, op-amps are commonly employed in a closed-loop configuration, wherein the output of the op-amp is fed back to the input through a feedback network. This feedback enables control over the gain, frequency response, and other properties of the circuit. Moreover, it enhances the stability and performance of the op-amp, addressing the issues related to its open-loop behavior.

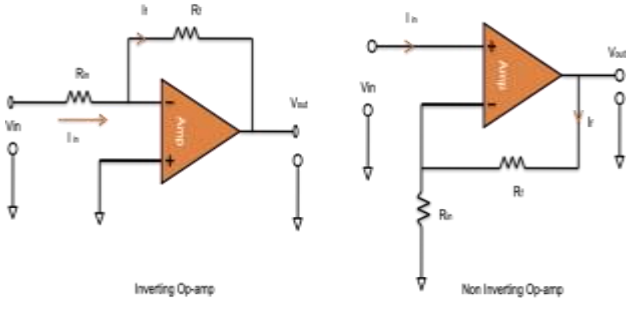


Fig. 2 Inverting and Non-Inverting Op-Amp

2.2 Difference amplifier

In analog-to-digital converters (ADCs), a difference amplifier is an operational amplifier (op-amp) circuit frequently utilized to amplify the disparity between two input signals. In an ADC, a difference amplifier serves as a preamplifier to magnify the small analog input signal prior to its processing by the remaining ADC circuitry. The difference amplifier encompasses two input terminals, a non-inverting input (+) and an inverting input (-), as well as two output terminals, an output voltage and a reference voltage. The output voltage is directly proportional to the discrepancy between the voltages applied to the non-inverting and inverting inputs.

Typically, the reference voltage is set to half of the supply voltage to accommodate both positive and negative input signals.

The gain of the difference amplifier is determined by the ratio of the feedback resistor to the input resistor. Adjusting the values of these resistors allows for gain modification. A higher gain results in a greater amplification of the difference between the input signals. Subsequently, this amplified signal is fed into the remaining ADC circuitry, such as an integrator circuit and a comparator circuit, to convert the analog input signal into a digital output. The accuracy and linearity of the difference amplifier significantly impact the overall performance of the ADC. Therefore, the design of the difference amplifier must focus on minimizing offset voltage, noise, and distortion to ensure precise and reliable conversion of the analog input signal[12].

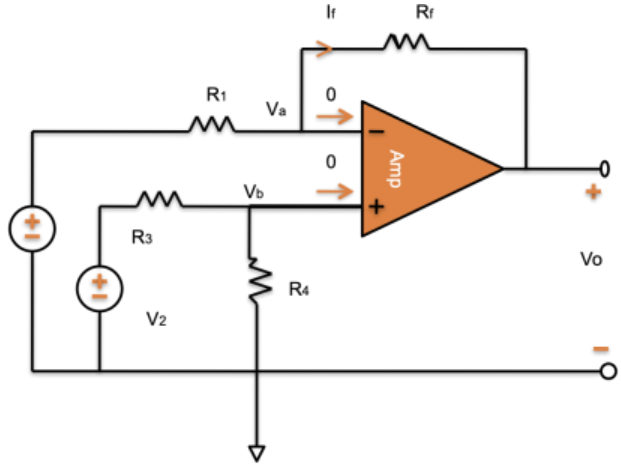


Fig. 3 Difference Amplifier

2.3 Integrator

An operational amplifier (op amp)-based integrator is a circuit that utilizes an operational amplifier to accomplish the task of integrating an input signal. It offers a straightforward and efficient method for integrating analog signals within electronic circuits. The fundamental setup of an op amp-based integrator comprises an op amp, a feedback capacitor, and a resistor. The input signal is applied to the non-inverting input of the op amp, while the output of the op amp is connected to the inverting input through a feedback capacitor. Additionally, a resistor is connected between the inverting input and ground.

Upon the application of an input voltage to the op amp- based integrator, the op amp amplifies the voltage and directs it through the feedback capacitor to the inverting input. The feedback capacitor serves as a storage device, accumulating charge over time. As the input voltage varies, the charge on the capacitor adjusts correspondingly. Consequently, the voltage across the capacitor is directly proportional to the integral of the input voltage.

The op amp-based integrator finds numerous practical applications, including audio signal processing, power electronics, and control systems. For instance, in audio signal processing, it can be utilized to implement a low- pass filter, effectively removing high-frequency noise from an audio signal. In power electronics, it enables the generation of a ramp waveform for pulse-width modulation (PWM) control circuits.

In control systems, it facilitates the implementation of a proportional-integral-derivative (PID) controller, commonly employed for regulating system output.

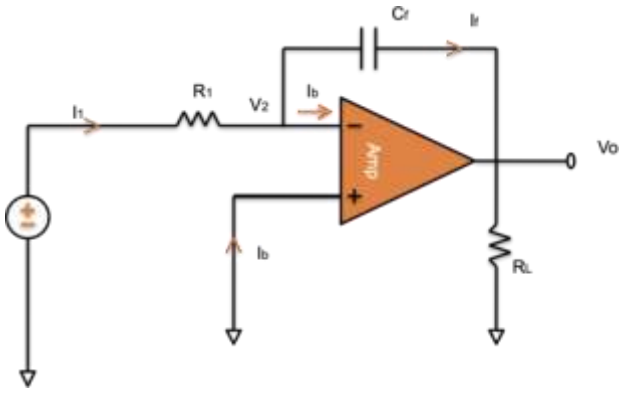


Fig. 4 Integrator

2.4 Comparator

A comparator is an electronic device designed to compare the amplitudes of two input signals and generate an output signal indicating which input is larger. Comparators find extensive application in electronic circuits for various purposes, including level detection, waveform shaping, and signal conditioning. The fundamental configuration of a comparator comprises two input terminals (positive and negative) and an output terminal. The input signals are applied to the respective input terminals, while the output terminal produces either a high or low voltage level based on the relative amplitudes of the input signals. The output of a comparator is binary, meaning it can be either high or low. When the voltage at the positive input exceeds that at the negative input, the output is high; conversely, when the voltage at the positive input is lower than that at the negative input, the output is low. This characteristic makes comparators valuable for detecting when an input signal crosses a specific threshold or for comparing two signals to determine their relative magnitudes.

Comparators are available in different types, including voltage comparators, current comparators, and time-domain comparators. Voltage comparators, the most commonly used type, compare the voltage levels of two input signals. Current comparators compare the current levels of two input signals, while time-domain comparators compare the time intervals between two input signals. Comparators find application in various fields, such as audio amplifiers, voltage regulators, and digital logic circuits. In audio amplifiers, comparators are employed to convert an analog audio signal into a digital signal by comparing it to a reference voltage. Voltage regulators use comparators to compare the output voltage to a reference voltage and adjust the regulator's output accordingly. In digital logic circuits, comparators are used to compare the voltage levels of two digital signals, generating a high or low output based on the relative voltage levels[13].

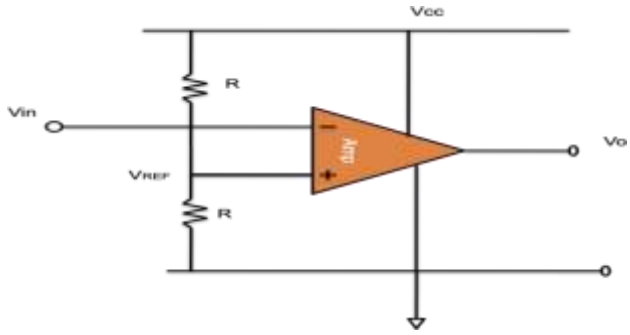


Fig. 5 Comparator

2.5 D flip flop

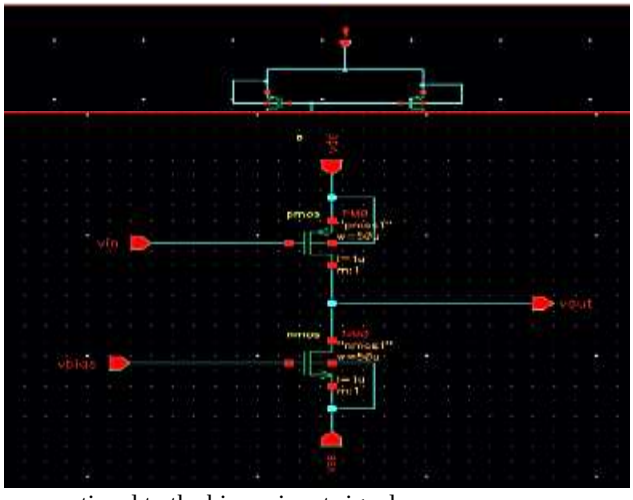
A D-Flipflp is a sequential logic circuit employed in a logical circuit employed in digital electronics and computer system to synchronize binary data, which can be represented as either a 0 or a 1. The D flip-flop possesses two stable states, determined by its input value, D. The output of the flip-flop, Q, mirrors its current state. During a transition of the clock input, CLK, from a low to a high level, the D input is sampled, causing the output to reflect the new value of D. The flip-flop maintains this state until the subsequent clock transition occurs. A D flip-flop typically consists of two NAND gates or two NOR gates connected in a feedback loop [14],[15]. One gate function as the input gate, while the other serves as the output gate. The input signal, D, is directed to one input gate, and the clock signal, CLK, is applied to the other input gate. The output, Q, is obtained from the output gate.

There exist two types of D flip-flops: level-triggered and edge-triggered. Level-triggered D flip-flops respond to the logic level of the clock input, causing the output to change when the clock input is maintained at a specific logic level. In contrast, edge-triggered D flip-flops respond to the transition or edge of the clock input, resulting in an output change only when the clock input transitions from one logic level to another [15]. D flip-flops find application in various digital systems like microprocessors, memory devices, and communication systems. They are utilized for storing data signals, synchronizing signals, and performing diverse control functions in digital systems. Additionally, D flip-flops can be employed to implement various types of sequential logic circuits such as shift registers and counters.

2.6 1 bit DAC

A Digital-to-Analog Converter (DAC) is an electronic device that transforms digital signals into analog signals. It finds widespread application in digital audio systems, control systems, and instrumentation to convert digital data into analog formats, enabling processing and output as voltage or current signals. The fundamental purpose of a DAC is to convert binary digital signals, such as pulse-code modulation (PCM) audio signals, into continuous analog signals[16]. This is accomplished by generating an output voltage or current that corresponds to the binary value of the input signal. Typically, the input signal is sampled at a fixed rate, and the output voltage or current is updated at the same rate to produce a smooth analog signal.

Various types of DACs exist, including resistor ladder, pulse-width modulation (PWM), sigma-delta, and current steering DACs. Resistor ladder DACs are the simplest and most commonly used, employing a network of resistors to generate an output voltage proportional to the binary input signal. PWM DACs utilize a digital pulse-width modulation technique to generate an analog output signal. Sigma-delta DACs employ a delta-sigma modulation technique, converting the input signal into a high-frequency bit stream that is subsequently filtered to produce a continuous analog signal. Current steering DACs generate a current output



proportional to the binary input signal.

DACs serve a wide range of applications, such as audio systems, control systems, and instrumentation. In audio systems, DACs convert digital audio signals into analog signals for amplification and sound reproduction. Control systems employ DACs to generate analog control signals for regulating various systems and devices. In instrumentation, DACs are utilized to generate precise analog signals used in testing and measurement endeavors[16].

3 RESULT AND ANALYSIS

Cadence was used to simulate both the individual components and the overall designed sigma delta modulator. Figure 6 to 16 illustrates the Schematic Diagram of the operational amplifier, differential amplifier, common source amplifier, difference amplifier, integrator, comparator, D flip-flop, 1-bit DAC, and sigma delta modulator respectively. The output gain of these components are shown in figure 17, 18, 19, 20, 21, 22, 23 and 24.

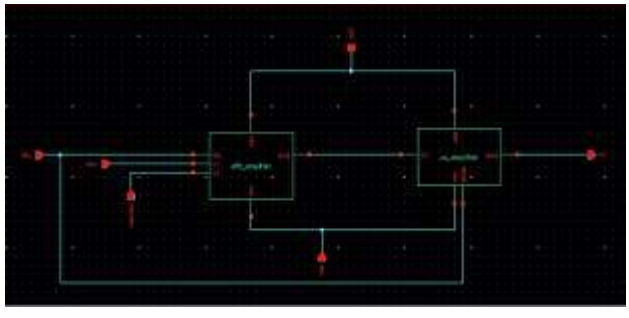


Fig. 6 Schematic Diagram of operational amplifier
Fig. 7 Schematic Diagram of differential amplifier
Fig. 8 Schematic Diagram of Common Source

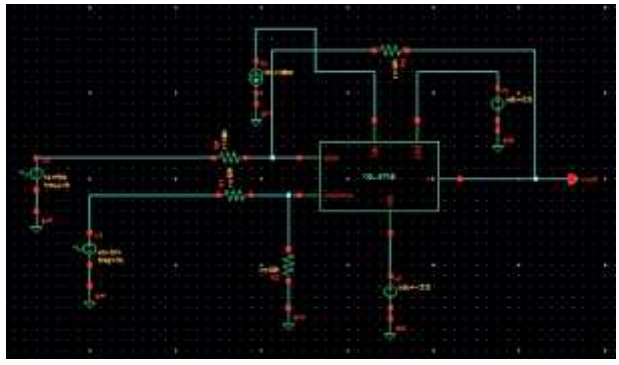


Fig.9 Schematic Diagram of difference amplifier

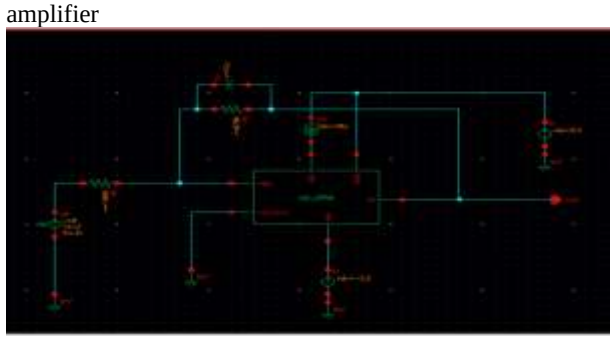


Fig. 10 Schematic Diagram of Integrator

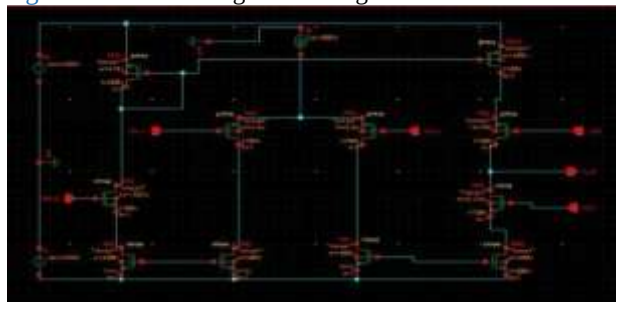


Fig. 11 Schematic Diagram of Comparator

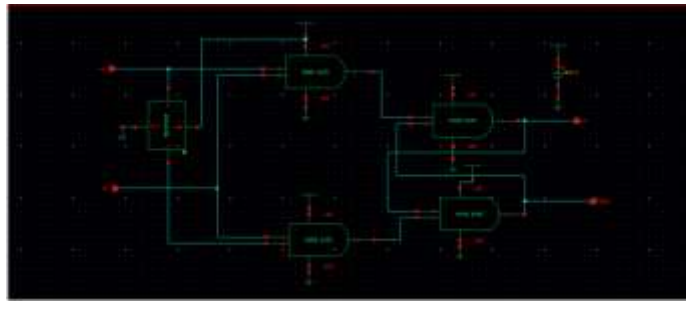


Fig. 12 Schematic Diagram of D flip flop

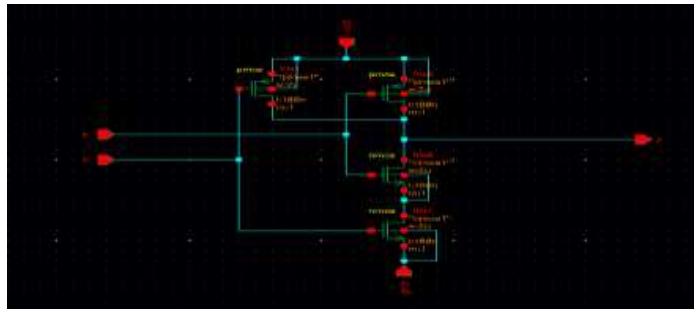


Fig. 13 Schematic Diagram of CMOS NAND gate

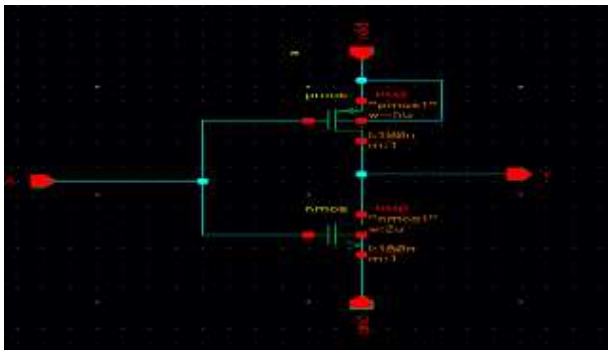


Fig. 14 Schematic Diagram of CMOS Inverter

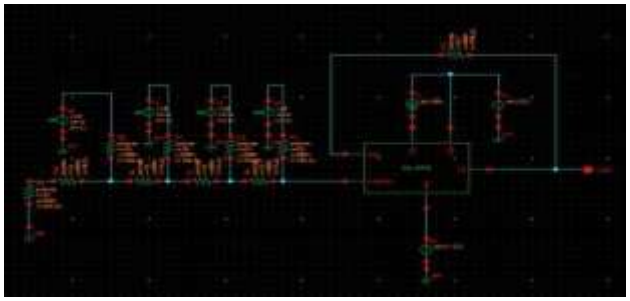


Fig. 15 Schematic Diagram of 4bit DAC

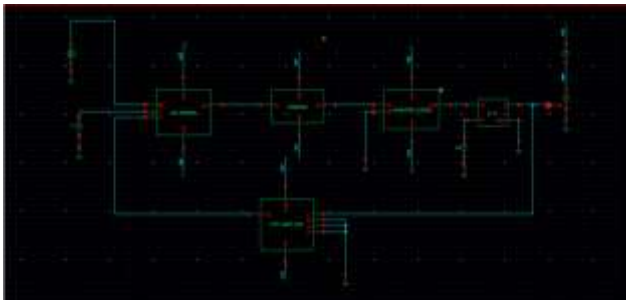


Fig. 16 Schematic Diagram of Sigma Delta Module

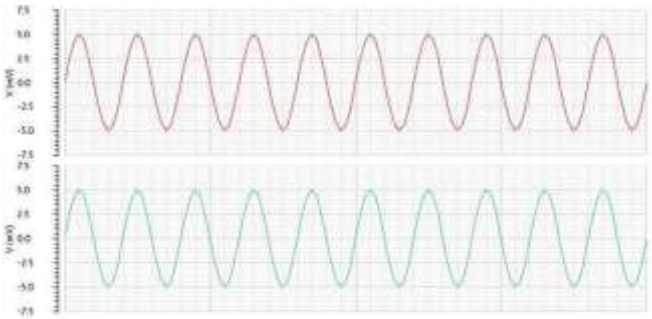


Fig. 17 Output gain of operational amplifier

Table. 1 Process simulation parameters of differential amplifier

Specifications	Results
DC gain(dB)	37.74023
Power Dissipation (mW)	1.009
CMRR(dB)	86.34234
Gain Bandwidth (MHz)	11.49834
Supply Voltage(V)	1.8

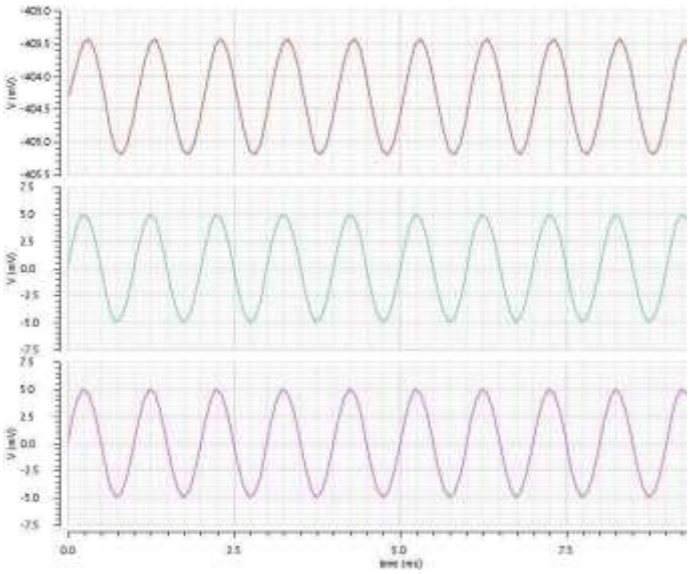


Fig. 18 Output gain of 2 stage operational amplifier

Table. 2 Process simulation parameters of 2 stage differential amplifier

Specifications	Results
DC gain(dB)	68.1577
Power Dissipation (mW)	1.009
CMRR(dB)	103.14903
Gain Bandwidth (MHz)	7.053154
Supply Voltage(V)	1.8

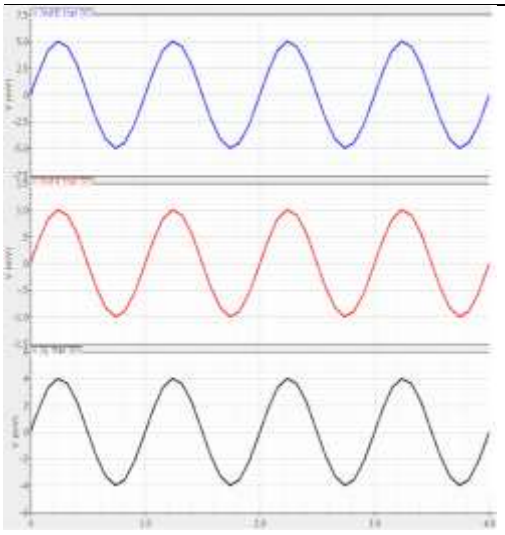


Fig. 19 Output result of difference amplifier

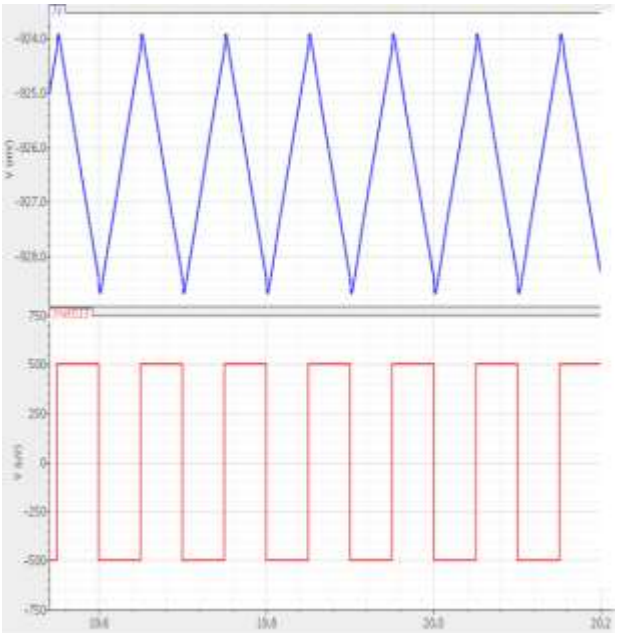


Fig. 20 Output result of Integrator

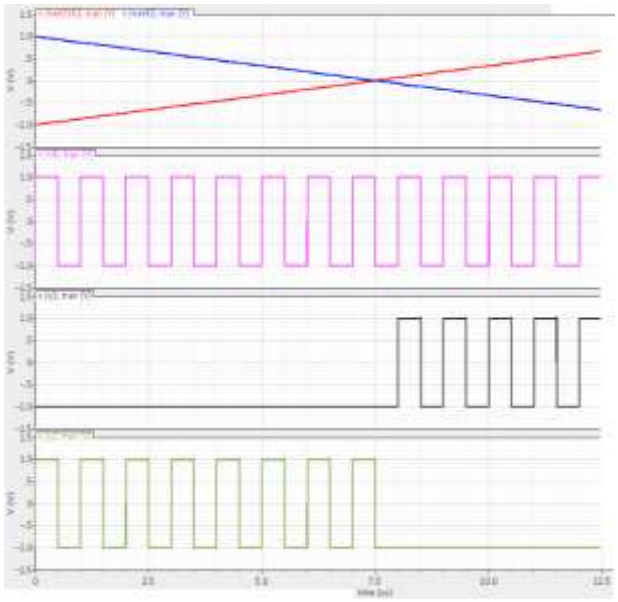


Fig. 21 Output result of clocked comparator

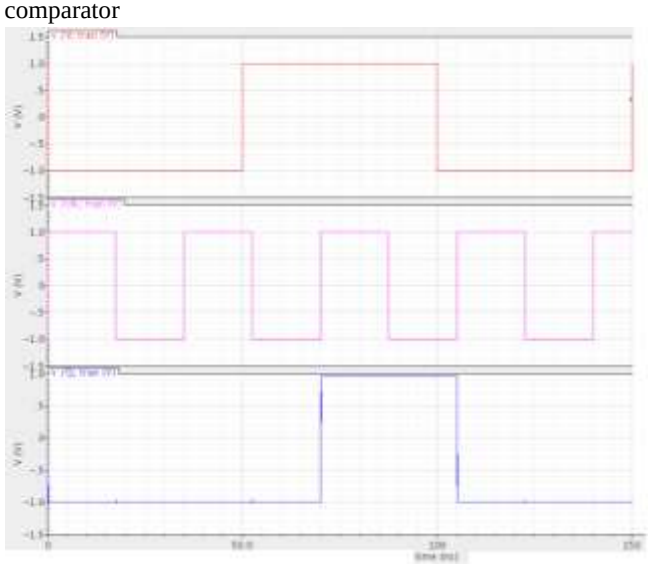


Fig. 22 Output result of D flip flop

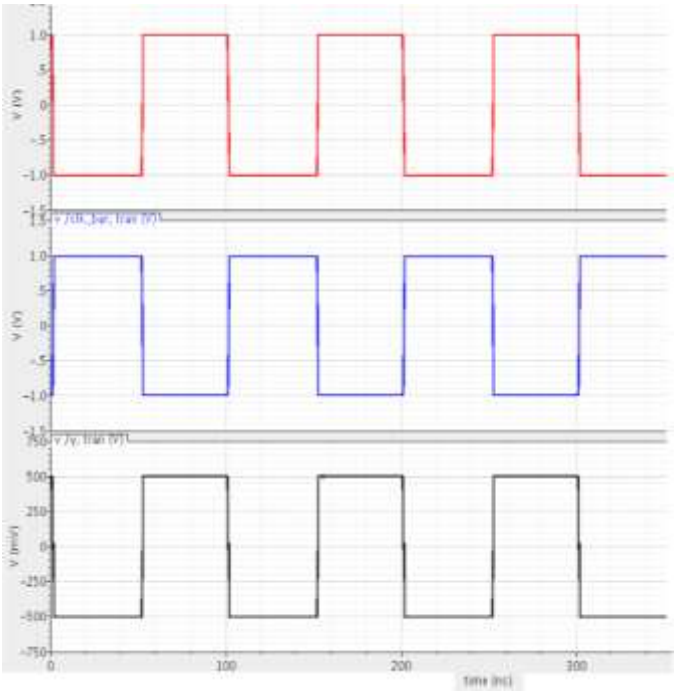


Fig. 23 Output result of 1 bit

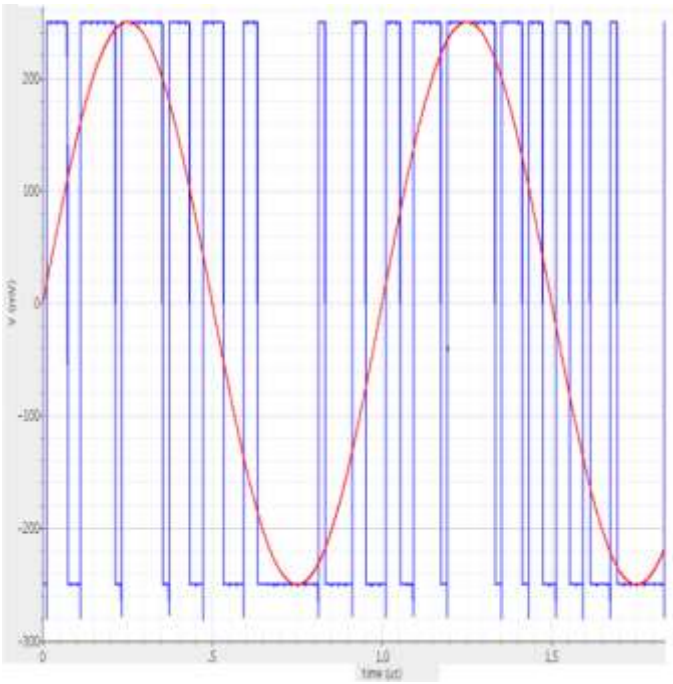


Fig. 24 Output result of Sigma Delta (ΣΔ) module

Table. 3 Comparison with Some Other Recent Work

Factor	[18]	[19]	[22]	[23]	This Work
Process Technology	130nm CMOS	180nm CMOS	0.18µm CMOS	0.35mm CMOS	180nm CMOS
Architecture	Sigma Delt	Sigma Delt	Sigma Delt	Sigma Delt	Sigma Delt

	a	a	a	a	a
Input Voltage	1V	2V	1V	3.3V	2.5V
SNR	78dB	---	85.2dB	85dB	6.2dB
Power dissipated	68µW	6.45µW	1.96mW	200mW	54µW

4 CONCLUSION

This paper offers a comprehensive overview of a highly energy-efficient sigma delta (ΣΔ) ADC modulator, specifically designed for aerospace applications in system-on-chip (SoC) Micro-Electromechanical Systems (MEMS) sensors. The research findings presented in this paper are compared in Table 3. Every aspect of the sigma delta (ΣΔ) ADC modulator is meticulously examined and modeled within this study. The proposed ADC modulator operates with remarkable efficiency, utilizing a minimal power supply range of +1.3V to -1.3V. Ata sampling frequency of 50 MHz, it consumes an average power of 54 µW.

REFERENCES

1. W. Yang, D. Kelly, I. Mehr, M. T. Sayuk and L. Singer (2001), A 3V 340mW 14b 75 Msample/s CMOS ADC with 85dB SFDR at Nyquist Input, IEEE Journal of Solid-State Circuits, 1931-1936, (Vol. 36). https://doi.org/10.1109/4.972143
2. S. Ardalan and J. Paulos (1987), An analysis of nonlinear behavior in delta - sigma modulators, in IEEE Transactions on Circuits and Systems, S. Ardalan and J. Paulos, An analysis of nonlinear behavior in delta - sigma modulators, in IEEE Transactions on Circuits and Systems, 593-603, (Vol. 34). https://doi.org/10.1109/TCS.1987.1086187
3. S. R. Norsworthy, R. Schreier and G. C.Temes (1996), Delta Sigma data converters: Theory, Design and Simulation, New York, IEEE press.
4. N. Mukahar and S. H. Ruslan (2012), A 93.36 dB, 161 MHz CMOS Operational Transconductance Amplifier (OTA) for a 16 Bit Pipeline Analog to Digital Converter (ADC), International Journal of Electrical and Computer Engineering (IJECE), 106-111, (Vol. 2).
5. M. Marufuzzaman, S. Z. Abidin, M. B. I. Reaz and L. F. Rahman (2014), Design of 3 bit ADC in 0.18µm CMOS Process, Telkomnika Indonesian Journal of Electrical Engineering, 5197-5203, (Vol. 12). http://doi.org/10.11591/tijee.v12i7.3618
6. Y. Fan, Y. Huijing and L. Gang (2013), A High Performance Sigma- Delta ADC for Audio Decoder Chip,Telkomnika, 6570-6576, (Vol. 11). http://dx.doi.org/10.11591/telkomnika.v11i11.3498
7. S. H. Ardalan and J. J. Paulos (1987), An analysis of nonlinear behaviour in delta sigma modulator, IEEE Trans. circuits and sys., 593-603, (Vol. 34). https://doi.org/10.1109/TCS.1987.1086187
8. R. Thankachan, K. R Jayakrishnan and T. K Shahana (2015), Design of 1 bit DAC for delta sigma modulator, Conference nternational on Emerging Trends in Technology and Applied Sciences, 19-22.
9. B. Razavi (1998), Design of CMOS Analog Integrated Circuits, McGraw Hill, California.
10. S. Chakraborty, A. Pandey, S. K. Saw and V. Nath (2015), A 6nW CMOS operational amplifier for bio-medical and sensor applications, Global Conference on Communication Technologies (GCCT), Thuckalay, 242-245. doi: 10.1109/GCCT.2015.7342659.
11. V. D. Kamath (2015), Overview of OP-AMP and OTA based integrators. International Journal of innovative research in electrical, electronics, instrumentation and control engineering, 74-81, (Vol. 3).
12. P. E. Allen and D. R. Holberg (2009), CMOS circuit design Oxford Indian Edition.
13. S. R. Norsworthy, R. Schreier and G. C. Temes (1998), Delta Sigma Data Converters: Theory, Design and Simulation, New York, IEEE press.
14. P. Kumar, J. Kaur (2017), Design of Various D Latch And Flop-Flop Using 180nm Technology, 06-07.
15. H. Joshi, S. M. Ranjan, V. Nath (2012) Design of High Speed Flip-Flop Based Frequency Divider for GHz PLL System:Technology, International Journal of Electronics and Computer Science Engineering, 1220- 1225, (Vol. 1).
16. S. M. Ranjan, V. Tiwari, V. Nath (2012), Design of Current Steering DAC for receiver in Wireless Communication, IJERT, ISSN 2278-0181/V7N1, 1260-1270.
17. C. Sandner, M. Clara, A. Santner,T. Hartig and F. Kuttner (2005). A 6-bit 1.2-GS/s low power flash ADC in 0.13 µm digital CMOS. IEEE Journal of Solid-State Circuits, 1499-1505, (Vol. 40).
18. K. L. Krishna, T. Ramashri and D. Reena (2014), A 1V second order delta sigma ADC in 130nm CMOS, International Conference on Information Communications and Embedded Systems.
19. H. Dosi and R. Agrawal (2013), Low power 8 bit analog to digital converter in 180nm CMOS technology, International Journal of Science and Research (IJSR), 417-418, (Vol. 2).
20. J. C. Candy (1986), Decimation for sigma delta modulation, IEEE Trans. Communication, 72-76, (Vol. 34).
21. Y. Shaojun, T. Ziquan, J. Yueming and D. Naiying (2013), The design of multi bit sigma delta ADC modulator, 2nd International Conference on measurement information and control, China, May.
22. M. A. Sohel, K. C. K. Reddy and S. A. Sattar (2012), Design of low power sigma delta ADC International Journal of VLSI design and communication systems, 67-80, (Vol. 3).
23. J. C. Morizio, M. Hoke, T. Kocak, C. Hughes, J. Perry, S. Madhavapeddi, M. H. Hood, G. L. H. Kondoh, T. Kumamoto, T. Okuda, H. Noda, M. Ishiwaki, T. Miki and M. Nakaya (2000), A 14 bit 2.2 MS/s sigma delta ADC, IEEE Journal of solid-state circuit, 968-976, (Vol. 35).

24. S. M. Ranjan, V. Tiwari, V. Nath (2013), Design of Current Steering Digital to Analog Converter using 250nm CMOS technology, IJECSE 2277-1956,1640-1650, (Vol. 1).
25. R. Kundu, A. Pandey, D. Gosh, J. Singh, V. Nath (2014), A 4.596 GHz, High slew rate, Ultra-low power, cascade operational amplifier in 45nm CMOS for wireless communication, International Journal of Computer Applications in Engineering Sciences, 15-20, (Vol. 3).
26. S. Chakraborty, A. Pandey, S. K.Saw and V. Nath (2015), A 6nW CMOS operational amplifier for bio-medical and sensor applications, Global Conference on Communication Technologies (GCCT), Thuckalay, 242- 245. doi: 10.1109/GCCT.2015.7342659.
27. A. Pandey, D. Yadav, R. Singh and V. Nath (2013), Design of Ultra Low Power CMOS Temperature Sensor of Space Applications, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 4117-4125, (Vol. 2).
28. A. Anand, B. Tudu, K. Datta, D. Prasad, S. Pal and V. Nath (2020), A 2 – 10 GHz Common Gate UWB Low Noise Amplifier in 90nm CMOS, International Science Exhibition Congress Symposium (SECS-2020) organized by IETE & ISVE Ranchi at ARTTC BSNL Ranchi.
29. V. Kumar, K. K. Singh, A. Pandey and V. Nath (2017), Design of Comparator in Sigma-Delta ADC Using 45 nm CMOS Technology, International Conference on Nano-electronics, Circuits & Communication Systems, Lecture Notes in Electrical Engineering, 381-387, (Vol. 403).
30. A. Pandey, M. J. Khan, D. Prasad, V. Nath, S. S. Solanki and L. K. Singh (2017), Switched Capacitor Circuit Realization of Sigma-Delta ADC for Temperature Sensor. International Conference on Intelligent Communication, Control and Devices. Advances in Intelligent Systems and Computing, 1129-1135, (Vol. 479).
31. D. Sharma, A. Rai, S. Debbarma, O. Prakash, M. K. Ojha and V. Nath (2023), Design and Optimization of 4-bit Array Multiplier with Adiabatic Logic using 65nm CMOS Technologies, IETE Journal of Research, https://doi.org/10.1080/03772063.2023.2204857.

AUTHORS

Jeet Tirkey is currently pursuing a B Tech degree in Electronics and Communication Engineering from Birla institute of Technology, Ranchi, Jharkhand, India. His areas of interest are low power VLSI design , digital VLSI design and signal processing.

Corresponding Author Email: jeettirkey643@gmail.com

Sarvesh Dwivedi is currently pursuing a B Tech degree in Electronics and Communication Engineering from Birla Institute of Technology, Ranchi, Jharkhand, India. His areas of interest are low power VLSI design and signal processing.

E-mail: sarveshdwivedi1212@gmail.com

Sanjay Kumar Surshetty received his BE degree in Electronics and Communication Engineering from Birla Institute of Technology, Mesra in 2020.He is working in Synopsys India PVT Limited as physical design engineer. His areas of interests are low power very large-scale integration design, Synthesis and ASIC Physical Design. E-mail: sanjaysurishetty@gmail.com

T. Snehitha Reddy received her BTech degree in Electronics and Communication Engineering from G. Narayanamma Institute of Technology and Science, Hyderabad, India in 2018, MTech in Electronics and Communication Engineering from Holy Mary Institute of Technology and Science, Hyderabad, India in 2021. She is pursuing a PhD degree in VLSI from Birla Institute of technology Mesra, Ranchi, India. Her areas of interest are low power very large-scale integration design, internet of things, artificial intelligence & machine learning, and computational intelligence.

E-mail: snehitha2206@gmail.com

Manoj Kumar received his PhD degree in Jan. 2019 from The North cap University Gurugram, India in Digital Image Forensics and MSc. from Institute of technology, Blanchardstown, Dublin, Ireland in 2013 and B.Tech degree from ITM University, India in 2008. His areas of interest are Image Processing, Digital Forensics, Image Processing and Information Security.
E-mail: wss.manojkumar@gmail.com

Vijay Nath received his BSc degree in physics from DDU University Gorakhpur, India in 1998 and PG diploma in computer networking from MMM University of Technology Gorakhpur, India in 1999 and MSc degree in electronic from DDU University Gorakhpur, India in 2001 and PhD degree in electronics from Dr. Ram Manohar Lohiya Avadh University Ayodhya, India in 2008. His areas of interest are low power very large-scale

integration design, ultra-low power complementary metal oxide semiconductor temperature sensors for missiles applications, microelectronics engineering, mixed signal design, application specific integrated circuit design, embedded system design, cardiac pacemaker, internet of things, artificial intelligence & machine learning, and computational intelligence.

E-mail: vijaynath@bitmesra.ac.in