ISSN: 2584-0495 Vol. 1, Issue 4, pp.195- 204

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

ASIC Design using Post Route ECO Methodologies for Timing Closure and Power Optimization

Akhil Sariki, Gatram Manoj Venkata Sai, Mamta Khosla, Balwinder Raj

Cite as: Akhil Sariki, Gatram Manoj Venkata Sai, Mamta Khosla, & Balwinder Raj. (2023). ASIC Design using Post Route ECO Methodologies for Timing Closure and Power Optimization. International Journal of Microsystems and IoT, 1(4), 195–204. https://doi.org/10.5281/zenodo.8402627

Published online: 25 September 2023.

DOI: https://doi.org/10.5281/zenodo.8402627

International Journal of Microsystems and IoT
Vol. 1, Issue 4, pp. 195-204; DOI: https://doi.org/10.5281/zenodo.8402627

ASIC Design using Post Route ECO Methodologies for Timing Closure and Power Optimization

Akhil Sariki[1], Gatram Manoj Venkata Sai[2], Mamta Khosla[1], Balwinder Raj[1]

[1] Department of Electronics and Communication Engineering, Dr. B R Ambedkar NIT Jalandhar, India.

[2] Department of Electronics and Communication Engineering, NIT Rourkela, India.

ABSTRACT

This paper presents work for timing and power optimization in ASIC in the post route phase. The current challenges of maintaining performance have led to research into alternative paradigms and complex design processes. Post-route design modifications are one of them and they are complex, time-consuming, and potentially disrupt physical synthesis, leading to routing bottlenecks and many other design issues. Fixing design constraints, verifying exhaustively, and reverting to synthesis stages can be time-consuming. This work discusses major post-route issues like electromigration, crosstalk, and antenna effects, as well as clock and Datapath optimization for timing closure. The work uses existing techniques to address these issues effectively by generating manual ECO, ensuring proper functioning of the chip, and promoting signal integrity all along the design process. This work also illustrated the effect of each step on the timing, power numbers and the cell utilization. Furthermore, the research has shown that harnessing existing traditional techniques, combined with a meticulous approach to selecting the optimal fixes through thorough verification, can significantly streamline the design signoff process.

KEYWORDS

Antenna effect; Cell characteristics; Crosstalk; ECO; Power optimization; Signal integrity; Timing closure; Verification

1. INTRODUCTION

The digital era, symbolized by the ubiquitous embracement of digital technology, has been significantly motivated by Moore's Law [1] and the exponential growth of VLSI design. Moore's law is the observation that the number of transistors in an integrated circuit (IC) doubles about every two years, which paved the avenue for the advancement of contemporary computers and electronic gadgets and made their use practical for the masses. Minimizing components, lowering prices, allowing technological convergence, and stimulating creativity across different disciplines has allowed interaction between Moore's Law and VLSI, which has not only fueled technical progress but also revolutionized the very fabric of civilization [2]. This progress is driven by the continuous scaling of integrated circuits, resulting in the introduction of lower technology nodes (such as 5nm, 3nm and 2nm), which became difficult to maintaining Moore's Law branched extensive research into other paradigms in the pursuit of further progress in the digital age [3][4]. Traditionally, ASIC design flows are used to design chips, and the processes comprise many steps [5]. In a typical design process, requirements and specifications come first, followed by architectural, logic [6], and physical design [7], and finally verification [8]. Subsequently, the process will proceed to production [9] and testing [10]. ASIC design turnaround times, however, have been continuously getting longer as an outcome of the rising complexity brought forth by frequent technical advancements [11]. With the progress in semiconductor technology come new challenges for designers, such as more complicated topologies, greater integration densities, and smaller transistor sizes [12]. These innovations call for sophisticated design methods [13][14][15], sophisticated toolkits [16], and rigorous verification techniques to guarantee functionality and dependability. As a result, it takes more time and energy to complete the design, verification, and production stages. With this new, longer schedule come new hurdles as designers try to keep up with the growing complexity of technological nodes without sacrificing the quality of their ASICs. In chip design, the post-route phase is a critical stage that follows the initial logical and physical synthesis of the design [17]. During this phase, the chip's physical layout, including the precise placement and routing of individual transistors and interconnects, is finalized to meet performance, timing, and manufacturing constraints, making it ready for fabrication. Post-route design modification implementation may be a difficult and time-consuming process [18]. These alterations have the potential to disturb the well-optimized balance attained through physical synthesis, which might have an impact on timing and introduce routing bottlenecks. Fixing design constraint violations is crucial, but it's a complex procedure. It is crucial to do exhaustive verification, which includes checking for logical correctness [19], timing [20], power usage, and more, but this may be time-consuming and resource intensive.

Iterations are prevalent; however, they increase expenses and the allocation of resources, which might influence the estimated duration and finances of a project. In addition, making alterations to the design by reverting to the synthesis or CTS stages may be laborious and time-consuming. The ripple effect of one change may need a lot of work to re-synthesize, re-optimize, and re-route. It is important to recognize that post-route design alterations, particularly those driven by high-level functional requirements or unforeseen circumstances, are a very common and often essential part of chip design, despite being generally avoided due to the potential for significant delays and complexity. Signal integrity and precise timing control are common victims of design modifications since they are crucial to the chip's proper functioning [20]. Typically, ECO approaches are used for addressing such violations in industry. Many strategies have been presented and are being used by the chip design community to address these issues [21][30]. These techniques include a broad variety of tactics and procedures, such as cutting-edge routing algorithms, optimization heuristics, and cell-type adjustments.

This work discusses the major post-route issues that need to be dealt with for design signoff. This includes signal integrity issues such as electromigration, crosstalk noise, and antenna effects, as well as clock and Datapath optimization for timing closure. Widely used methods for fixing these issues are discussed in the background section. In this context, the present work also puts forward a combined approach aimed at using existing techniques more effectively to achieve timing closure and uphold signal integrity throughout the chip design process.

2. Background

2.1 Timing Closure

Timing is quite a crucial and mandatory parameter of any processor design, during which great care is taken to be certain that the proposed integrated circuits adhere to strict timing restrictions and standards [22]. An important step towards timing signoff is STA. STA is used because it can test the timing features of any digital design in a thorough and methodical manner. It detects and measures possible timing violations, including setup & hold time violations, that are vital to the circuit's accurate and dependable operation. By highlighting crucial timing pathways and endpoints, STA not only aids in the optimization process but also allows engineers to zero in on precisely what needs fixing. STA is a vital element of the sign-off process because it validates that the designed chips meet their timing parameters before entering production. Data and clock paths are optimized with the help of swapping, sizing and buffer insertion [30] to meet the timing requirement of the device.

2.2 Signal Integrity

VLSI design relies heavily on signal integrity, which outlines the consistency and reliability of signals as they travel between different parts of a processor. This includes things like reliability and the capacity to keep data intact throughout transmission. In high-speed and high-frequency applications it is imperative to maintain high signal integrity to facilitate the accurate operation of electronic systems and the error-free transmission of data.

2.2.1 Crosstalk

Crosstalk in VLSI is any phenomenon in electronics that occurs when a signal carried on one circuit or channel of a transmission system causes an undesirable effect in another circuit or channel. Crosstalk is typically generated by unwanted capacitive, inductive, or conductive coupling between circuits or channels. As component densities rise and feature sizes diminish, interconnects must be placed closer together than ever before in contemporary semiconductors, making this a very important issue. Without adequate management, crosstalk may have a negative impact on an IC's performance and reliability. In any chip design, timing signoff is typically achieved by taking crosstalk effects into account. Timing constraints must be met, and designers must take crosstalk-induced delays into consideration. Shielding and enough space between signal paths are both necessary to reduce capacitive crosstalk. Crosstalk-induced latencies can be reduced by just inserting buffers at the violating endpoint [20][30]. Proper routing [24] and strategic placement [25] of key signals may further reduce crosstalk effects, ensuring the overall effectiveness and reliability of ICs in the processor design.

2.2.2 Electromigration

Electromigration is the movement of atoms based on the flow of current through a material. If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them. The structural faults produced by this process can break conductor continuity, increase resistance, overheat, and lead to open circuits or shorts [26]. Manufacturers of semiconductors respond to this challenge by increasing metal widths, tweaking supply voltage, shortening metal length or by resizing the buffer [27]. Predicting and avoiding reliability concerns in processor design requires accurate modelling and simulation of electromigration processes. Refining and validating electromigration

models relies heavily on post-silicon validation findings since they give real-world data that can be used to calibrate the models' accuracy.

2.2.3 Antenna Effect

During the fabrication process, we need to etch out the unwanted oxide layer from the wafer, which can be done using plasma etching. The gates of transistors and metal pin connections can act like antennas and build up charges when exposed to ionizing radiation. which may lead to permanent damage to the device gate oxide. VLSI designers may use diode structures to deflect the accumulated charge away from the chip's vulnerable areas, lessening the impact. The antenna rule is provided by Foundry which must be followed during the layout design. The antenna effect may be mitigated further with thoughtful routing known as jogging/hopping or by reducing the via size [28].

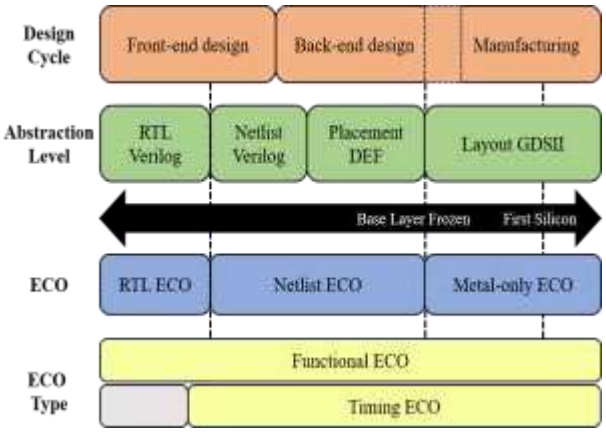


Fig. 1 ECO types and occurrence during the design cycle [23]

2.3 ECO (Engineering Change Order)

Engineering Change Order or ECO in VLSI is used to accommodate last-minute design revisions in the processor and this is often used to fix design flaws, improve speed/performance, or include new salient features. These improvements are iterative and economical. Multiple ECO iterations are performed after the first implementation and are a standard part of the processor design cycle. Functional, timing, power, yield, physical, and DFM ECOs are several possible forms of ECOs [29]. Fixing bugs, adding new features, and upgrading present ones are a multitude of functional ECOs. The intent of timing ECOs is to optimize the design's timing performance by doing things like upgrading cell drive sizes and enhancing critical timing paths. Voltage scaling and network optimization are two examples of power ECOs' energy-saving goals. By addressing issues caused by process variability or poor architecture, yield ECOs aim to increase production output. Changing the actual implementation of a design, such as by relocating cells or rerouting networks, is an example of a physical ECO. DFM ECOs aim to increase the design's manufacturability by fixing problems with mask generation, lithography, and several other problems in manufacturing. They may happen at any point in the processor design cycle, right from the very first tape out through the last round of silicon validation. After generating the ECO file for the fixes, they start applying it to the PnR database where the analysis was done.

3. TIMING CLOSURE METHODOLOGY

This section discusses streamlined signal integrity and timing closure methodologies with the help of the existing solutions discussed in literature. It delves into antenna effect and crosstalk optimization for signal integrity and clock and Datapath optimization for timing closure using prior existing techniques [30]. On top of this, power optimization was also performed on the over-fixed timing paths for good power numbers.

3.1 Antenna Effect optimizations for Signal Integrity

A well-structured approach is used to minimize this antenna effect systematically. During the preliminary phase, the design is thoroughly examined in order to identify pins that have a noticeable gate length-to-metal route ratio. After identifying probable antenna breaches, the analysis proceeds to assess the degrees of congestion in the bottom metal-layer and the neighboring layer around the victim cell. If the assessment indicates that there is little congestion in the impacted regions, a method known as "metal hopping" is used. The purpose of these modifications is to implement alterations or variations in the route with the objective of mitigating the susceptibility to the antenna effect. In situations where the act of jogging along the designated path fails to rectify the violation of the antenna effect, a more thorough analysis is necessary. One potential solution is the implementation of a diode cell to address the issue at hand. The positioning of the diode cell is carefully implemented to promote the dissipation of plasma-induced charges. The use of a diode cell enhances the circuit's resilience and its capability to properly manage charge accumulation. The proposed approach places more emphasis on metal hopping or jogging as compared to diode insertions as the principal strategy for mitigating antenna impact concerns. The intent is to minimize the need for diode insertion. This strategy serves the dual purpose of simplifying the design by minimizing the no. of additional components and addressing the issue of possible cell congestion. By

adhering to this methodology, designers can methodically identify, assess, and address antenna effect concerns within their designs.

3.2 Crosstalk optimizations for signal integrity

Figure. 2 illustrates how a systematic approach of existing techniques can effectively deal with crosstalk noise. The gravity of the violation may be gauged from this background. The process prioritizes violations in accordance with delta values, which measure the degree to which a specific net is disrupted by crosstalk. Delta levels larger than the acceptable limit indicate more severe infractions that need quick attention. The procedure finds all relevant route shapes that are vulnerable to crosstalk for each high-delta crosstalk violation.

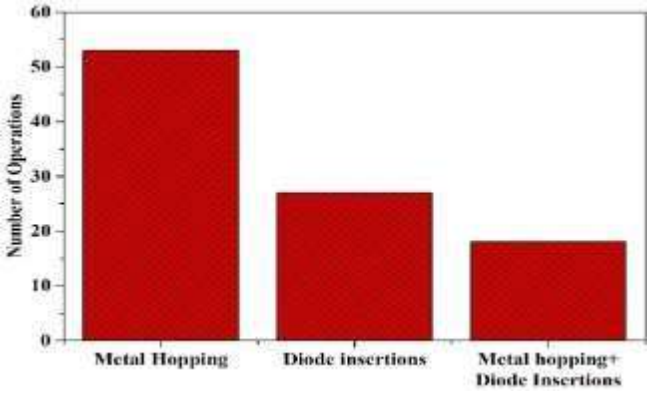


Fig. 2 Number of various antenna effect optimizations

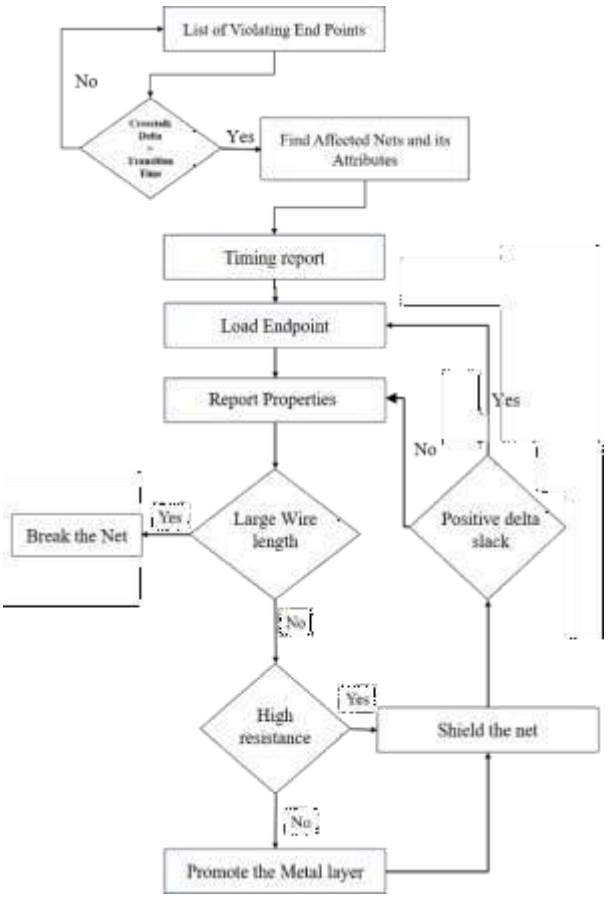


Fig. 3 Crosstalk optimization for signal integrity in design

(i) If the route length of the shape of a particular net is too large, a smart strategy is to include a buffer element somewhere in the center of the net. By decreasing the transition latency over long, high-resistance channels, this helps to mitigate crosstalk. In contrast, route attributes are investigated once the net length is noted below the assigned threshold. (ii) The possibility of advancing the net to upper routing layers is considered if the route is already located on lower metal levels. Since the top metal layers have low resistance and greater capacitance owing to their widened widths, this elevation is intended to reduce.
route latency. (iii) Shielding techniques are used on these redirected nets to diminish the cross-cap value because it is a major cause of net delay. This method improves the reliability of signals and reduces the negative effects of crosstalk by decreasing the coupling cross capacitance among the intended target and aggressor networks in a productive way. Because of the signal integrity fixes timing gets better but in some cases it deteriorates.

3.3 Data path Optimization for timing Closure

Timing closure issues can be resolved in a wide variety of ways. However, the relationship between setup-violating paths and the synthesized clock enables the possibility of modifying it via the clock modifications. Addressing hold/min violations is a key aspect to consider since it requires a sufficient slack margin in the hold-violating path to allow buffer insertion. Attaining a credible and accurate design requires the careful calibration of data and clock latencies to maintain an optimal balance. The requisite steps for solving timing via Datapath improvements are described and a comprehensive synopsis of the approach is provided. (i) Obtaining timing information for every non-compliant endpoint is a crucial first step. The comprehensive timing report provides essential information pertaining to the timing features of the framework, including various delays, design constraints, and clock attributes. This report serves as an invaluable resource for the identification and resolution of timing-related problems. (ii) Search for instances of minimum delay path, maximum delay path, and min-max delay path violations. (iii) Identify all high VT cells inside the data-path in cases where the violation corresponds with the max-path, indicating that the endpoint experiences excessive data propagation time. It's known that a high VT cell's large

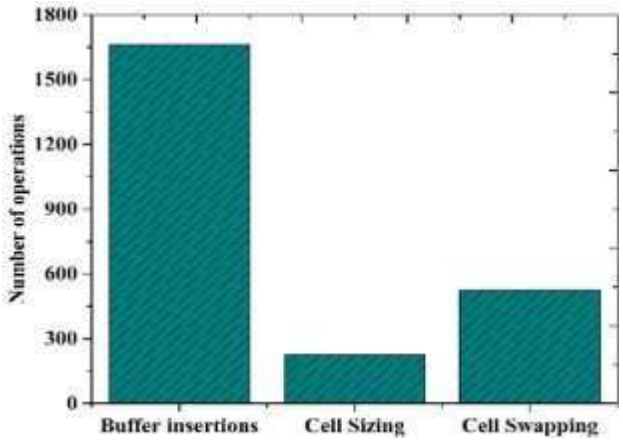


Fig. 4 Number of Datapath optimizations on timing path

threshold voltage causes it to switch states slowly, adding to the total latency. (iv) The implemented flow includes a method for swapping a high VT cell with a low VT cell if there are high VT cells situated in the layout. The fundamental aims of this operation are to enhance overall timing performance and minimize delays. When determining the sequence for cell swapping, it is advisable to choose a high VT cell that exhibits a low-fanout, high-transconductance, and high cap. To significantly minimize disturbances in other logical paths due to swapping, the implementation should take the hold margin of the data-path into account. If the max-path slack is deemed favorable, indicating that the path now meets the timing conditions, the flow will proceed to the subsequent endpoint. If the slack remains negative, implying that the desired timing has not yet been achieved, the flow reverts and verifies the existence of further high VT cells in order to repeat the previous step. The previously repeated process stays in place till the violation has been rectified. The flow adopts an alternative strategy to resolve the violation in cases of the absence of high VT cells (i.e., regular VT cell count equals zero), rendering swapping unfeasible. (v) Examine cells exhibiting diminished drive size, which are indicative of suboptimal driving capabilities and consequent amplification of delay. In a manner akin to cell swapping, choose a cell with a relatively small drive size and increase its capacity. Subsequently, flow resolves timing violations corresponding with the delay requirement. (vi) Similarly, for mine-path violations, a special hold buffer is inserted at the point of termination to aid in hold-related violations if ample max slack is available. In modern digital designs, the adoption of various methods such as regular VT cell switching, cell upsizing, and buffer inclusion is prevalent to enhance timing and accomplish the envisioned performance targets. But timing concerns need to get handled systematically because of their repetitive nature, with a certain priority devoted to the most severe violations. If a max violation results in negative slack, the subsequent analysis explores several alternatives for rectifying the max-path violation. In scenarios where the previous procedures are ineffective, sometimes it is vital to pinpoint the specific violation and resort to alternative approaches for addressing the violation. These targeted solutions facilitate the resolution of the breaches and assure that the overall layout is consistent with the design objectives. Table 1 show Impact of Datapath optimization on Timing.

Table. 1 Impact of Datapath optimization on Timing

Parameter	Before timing fixes	After timing fixes
Setup timing (WNS/TNS/NVP)	-93.596/-15071.632/915	-58.857/-652.3698/85
hold timing. (WNS/TNS/NVP)	-80.520/-194789.320/3200	0/0/0

3.4 Clock path Optimization for timing Closure

Clock path optimization focuses on addressing violations that can't be adequately addressed through optimizing data path alone. In this method, we meticulously manipulate the clock-build tree network to introduce intentional skew in the clock's traversing timing path using delay components like clock inverters and buffers. The objective here is to push the clock for skew adjustments from ports to design for rectifying given timing violation. However, it's important to note that accomplishing the expected clock skew isn't always straightforward. In cases where the ideal skew can't be achieved, the clock-build tree network employs an iterative process that involves the gradual introduction of inverter pairs in the clock's traversing timing path from terminals to registers. These inverters are strategically modified to fine-tune the clock skew by pushing to a distance or adding a pair in a certain distance. The pushing distance depends on the criticality of the setup violations. It's worth noting that while clock path optimization can be effective in addressing specific violations, it might introduce additional violations that are addressable in a single iteration. Table. 2 shows, Impact of clock path optimization on Timing.

Table. 2 Impact of clock path optimization on Timing

Parameter	Before timing fixes	After timing fixes
Setup timing (WNS/TNS/NVP)	-58.857/-652.3698/85	-17.322/-3.212/14
hold timing. (WNS/TNS/NVP)	0/0/0	946.638/-8.371/166

To achieve comprehensive timing closure, design teams often employ a hybrid approach that optimizes both paths related to clock and data. After another round of timing fixes it can be observed that over timing is closed with respect to both setup as well as hold design constraints. Figure 6 depicts the overall timing numbers in every stage of timing optimization.

3.5 Optimizing Power in Timing Paths

The utilization of low-voltage threshold cells was significantly enhanced when an optimistic timing fix technique was first used to alleviate setup violations. However, this culminated in a significant increase in energy usage. Later, a partly pessimistic timing approach was employed to find an optimum medium between area utilization, performance/speed, and power. Its major goal was to pinpoint possible power-saving opportunities in the circuit timing paths without compromising performance. Within this approach, emphasis was placed on paths that provided ample setup slack. In these cases, regular VT cells were methodically substituted for the low-voltage threshold

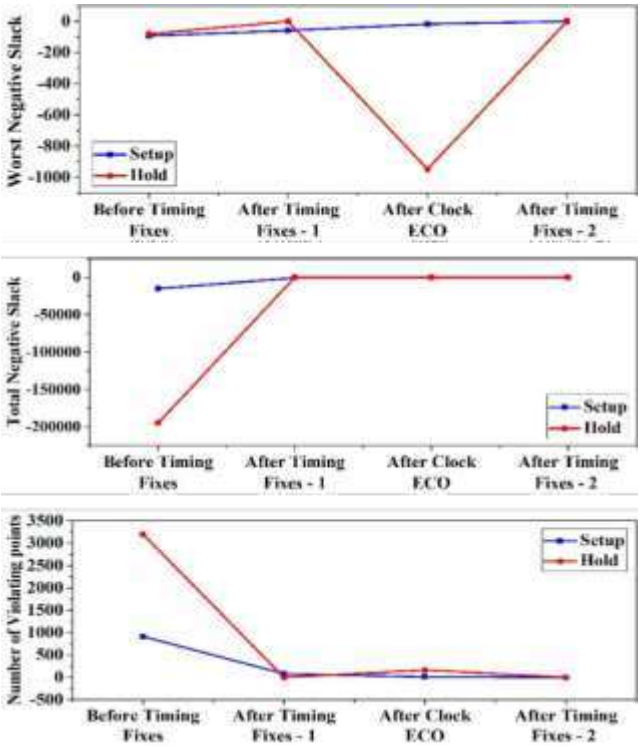
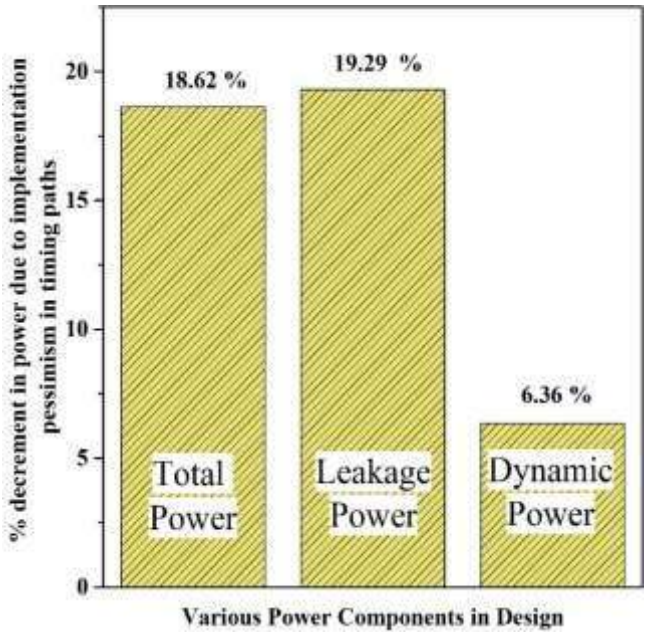


Fig. 5 Overall Timing numbers in various stages of implementation.

cells [31]. This is Centered on the observation that regular VT cells suffer less power loss as an outcome of leakage current, which drives the cell switching from low voltage threshold cells to them, power settings are optimized to show significant improvements, which are graphically illustrated in Figure 4. This strategy achieves a fair compromise by replacing low-VT cells with [32] regular voltage threshold cells only along timing pathways with sufficient slack. This strategy efficiently optimizes power consumption without losing the ideal device operation. It's a good model of the delicate balance that must be struck between improving performance and conserving power that the results circuit is both powerful and efficient.



3.6 Comparative chip analysis with and without ECO.

After Engineering Change Orders (ECOs) have been implemented, the chip's overall performance is evaluated, with a focus on power, performance, and area (PPA). Figure 7 is a visual representation of this analysis. It shows how the PPA parameters of the chip changed before and after the deployment of ECO, with a focus on how much each parameter changed. The maximum attainable clock frequency has increased significantly, by 8.3%, which is a significant improvement in terms of performance. This is indicative of a significant increase in the chip's

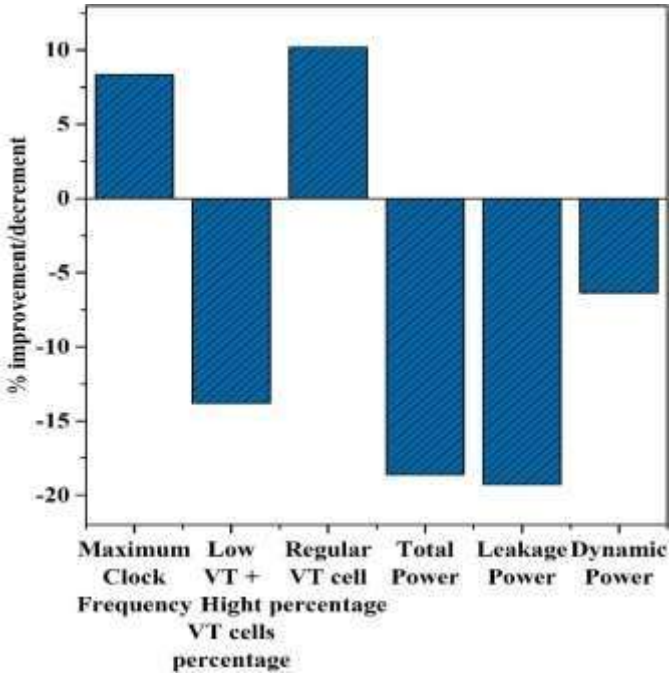


Fig. 7 Comparative chip analysis with and without ECO Overall design improvement summary with respect to power area and performance

operating speed, which may result in enhanced overall performance across a range of applications. Power efficiency is being tackled from several angles. All the chip's power-related subsystems have been upgraded. Low and high VT (threshold voltage) cells have been used 13% less often, which is a significant decrease. Together, these improvements cut power usage by an astonishing 18%. These enhancements not only help the chip use less energy, but they might also increase its durability and reliability. Overall, the post-ECO review demonstrates significant improvements in both performance and power economy, elevating the chip's standing as a viable option for a wider variety of uses.

4. Conclusion

In summary, this research paper has delved into the critical, multifaceted challenges encountered in the post-route phase of chip design. The important consequences of issues with signal integrity, such as antenna effects and crosstalk, have been addressed. In addition, the study has investigated timing closure through careful optimizations of data and clock paths, giving readers an understanding of the complexities involved in attaining exact timing control by traditional, systemic methods. This study has provided a comprehensive overview of the ECO implementation process by detailing the timing numbers at each step. In addition, the research has investigated efficiency gains by investigating the effects of cell features on time paths. The study shows the percentage reduction in each power component because of these optimizations, providing quantitative evidence of the gains made. The report concludes with a synthesis of all the results, including a thorough discussion of the factors governing power, performance, and area. The study also shows that the design signoff process may be greatly streamlined by making use of current conventional approaches in conjunction with a diligent approach to picking the ideal fixes through comprehensive verification. This method not only speeds up the design approval process but also makes better use of available resources. It is worth acknowledging that, right now, all ECOs are manually generated. In the future, there is a potential possibility for the automation of this process, which could further streamline and accelerate post-route design signoff.

REFERENCES

1. G. E. Moore, (1996), Intel: Memories and the Microprocessor. Daedalus, 55–80, (Vol. 125). http://www.jstor.org/stable/20013439
2. G. D. Hutcheson, (2009), The Economic Implications of Moore's Law, Into the Nano Era, 11–38. https://doi.org/10.1007/978-3-540-74559-4_2
3. H. N. Khan, D. A. Hounshell, and E. R. H. Fuchs, (2018), Science and research policy at the end of Moore's law, Nature Electronics, 14–21, (Vol. 1). https://doi.org/10.1038/s41928-017-0005-9
4. J. Shalf, (2020), The future of computing beyond Moore's Law. Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences, 20190061, (Vol. 378). https://doi.org/10.1098/rsta.2019.0061
5. V. Taraate, and V. Taraate, (2021), ASIC Design Flow. ASIC Design and Synthesis: RTL Design Using Verilog, 13-26.
6. J. Rodrigues, M. Kamuf, H. Hedberg, and V. Owall (2005), A Manual on ASIC Front to Back End Design Flow, Proc. IEEE International Conference on Microelectronic Systems Education (MSE'05). https://doi.org/10.1109/mse.2005.9
7. A. Amid, D. Biancolin, A. Gonzalez, D. Grubb, S. Karandikar, H. Liew, A. Magyar, H. Mao, A. Ou,

N. Pemberton, P. Rigge, C. Schmidt, J. Wright, J. Zhao, Y.S. Shao, K. Asanovic, and, B. Nikolic, (2020), Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs. IEEE Micro, 10–21, (Vol. 40). https://doi.org/10.1109/mm.2020.2996616

8. S. Kim, S. Y. Lee, S. Park, K. R. Kim, and S. Kang, (2020), A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 3138–3151, (Vol. 67). https://doi.org/10.1109/tcsi.2020.2990748
9. M.Wasim, P. V. Serra, and T. D. Ngo, (2020), Design for manufacturing and assembly for sustainable, quick and cost-effective prefabricated construction – a review. International Journal of Construction Management, 3014–3022, (Vol. 22. https://doi.org/10.1080/15623599.2020.1837720
10. G. N. Balaji, and S. C. Pandian, (2019), Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates, Cluster Computing, 15231-15244, (Vol. 22). https://doi.org/10.1007/s10586-018-2552-x
11. T. Pirson, T. P. Delhaye, A. Pip, G. L. Brun, J. P. Raskin, and D. Bol, (2022), The environmental footprint of ic production: Review, analysis and lessons from historical trends, IEEE Transactions on Semiconductor Manufacturing. https://doi.org/10.1109/tsm.2022.3228311
12. G. Moody, V. J. Sorger, D. J. Blumenthal, P. W. Juodawlkis, W. Loh, C. S. Agaskar, and R. M. Camacho, (2022), 2022 roadmap on integrated quantum photonics, Journal of Physics: Photonics, 012501, (Vol. 4). https://doi.org/10.1088/2515-7647/ac1ef4
13. K. Zhu, C. Wen, A. A. Aljarb, F. Xue, X. Xu, V. Tung, and M. Lanza, (2021), The development of integrated circuits based on two-dimensional materials, Nature Electronics, 775-785, (Vol. 4). https://doi.org/10.1038/s41928-021-00672-z
14. M. S. K. Pheng, and L. G. David, (2022), Artificial intelligence in back-end semiconductor manufacturing: A case study, Proc. 2022 IEEE International Conference on Distributed Computing and Electrical Circuits and Electronics (ICDCECE), IEEE, 1-4. https://doi.org/10.1109/ICDCECE53908.2022.9792976
15. J. Senoner, T. Netland, and S. Feuerriegel, (2022), Using explainable artificial intelligence to improve process quality: Evidence from semiconductor manufacturing, Management Science, 5704-5723, (Vol. 68). https://doi.org/10.1287/mnsc.2021.4190
16. K. I. Gubbi, S. A. Beheshti-Shirazi, T. Sheaves, S. Salehi, S. M. PD, S. Rafatirad, and H. Homayoun, (2022), Survey of machine learning for electronic design automation, Proc. Great Lakes Symposium on VLSI 2022, 513-518. https://doi.org/10.1145/3526241.3530834
17. N. Danthamala, V. Das, and V. Hanchinal, (2023), Digital Backend Optimization Techniques for Post-Route and Sign-Off Challenges in ASIC Design, Proc. Second International Conference on Computational Electronics for Wireless Communications: ICCWC 2022, 359-368. Singapore: Springer Nature Singapore. https://doi.org/10.1007/978-981-19-6661-3_32
18. S. Saurabh, (2023), Introduction to VLSI Design Flow, Cambridge University Press.
19. E. Seligman, T. Schubert, and M. A. K. Kumar, (2023), Formal verification: an essential toolkit for modern VLSI design, Elsevier.
20. S. Saurabh, H. Shah, and S. Singh, (2018), Timing closure problem: Review of challenges at advanced process nodes and solutions, IETE Technical Review. https://doi.org/10.1080/02564602.2018.1531733
21. Y. C. Fan, Q. Yu, T. Schumann, Y. R. Chien, and C. C. Lu, (2014), Advanced VLSI architecture design for emerging digital systems. VLSI Design, 2014, 1-2. https://doi.org/10.1155/2014/746132
22. R. N. Bhukya, and R. Mudavath, (2019), Analysis and minimization of crosstalk noise in copper interconnects for high-speed VLSI circuits, CSI Transactions on ICT, 81-86, (Vol. 7). https://doi.org/10.1007/s40012-019-00243-w
23. I. H. R. Jiang, and H. Y. Chang, (2011), ECOS: Stable matching-based metal-only ECO synthesis, IEEE transactions on very large scale integration (VLSI) systems, 485-497, (Vol. 20). https://doi.org/10.1109/TVLSI.2011.2104377
24. R. Liang, Z. Xie, J. Jung, V. Chauha, Y. Chen, J. Hu, and G. J. Nam, (2020), Routing-free crosstalk prediction, Proc. of the 39th International Conference on Computer-Aided Design 1-9. https://doi.org/10.1145/3400302.3415712
25. Y. Qiu, Y. Xing, X. Zheng, P. Gao, S. Cai, and X. Xiong, (2023), Progress of Placement

Optimization for Accelerating VLSI Physical Design. Electronics, 337, (Vol. 12). https://doi.org/10.3390/electronics12020337

26. S. Bigalke, and J. Lienig, (2020), Avoidance vs. repair: New approaches to increasing electromigration robustness in VLSI routing. Integration, 189-198, (Vol. 75). https://doi.org/10.1016/j.vlsi.2020.04.009
27. Majji, Sankararao, et al. (2020), A Study on the Comprehensive Analysis of Electro Migration for the Nano technology trends, Proc. 6th International Conference on Advanced Computing and Communication Systems (ICACCS). IEEE. https://doi.org/10.1109/ICACCS48705.2020.9074328
28. R. K. Pandey, E. F. Pribadi, and P. C. P. Chao, (2022), Technology scaling impact on VLSI interconnect and low swing signaling technique. Microsystem Technologies, 2337-2351, (Vol. 28). https://doi.org/10.1007/s00542-022-05329-1
29. S. Rangarajan, P. Chakrabarti, S. Sahais, A. Datta, and A. Subramanya, (2014), Tutorial T3B: Engineering Change Order (ECO) Phase Challenges and Methodologies for High Performance Design, Proc. 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems IEEE, 7-8. https://doi.org/10.1109/VLSID.2014.118
30. A. Sharma, and S. Deb, (2015), Smart and efficient multi-scenario SoC timing closure and ECO generator (PG dissertation).
31. M. Maiti, S.K. Saw, V. Nath, A. Majumdar, (2019), A power efficient PFD-CP architecture for high-speed clock and data recovery application, Microsystem Technologies, Springer Berlin Heidelberg, 4615-4624, (Vol. 25). https://link.springer.com/article/10.1007/s00542-019-04458-4
32. D. Prasad D. V. Nath (2018), An ultra-low power high-performance CMOS temperature sensor with an inaccuracy of -0.3oC/ +0.1oC for aerospace applications, Microsystem Technologies, Springer Berlin Heidelberg,1553-1563, (Vol. 24). https://doi.org/10.1007/s00542-017-3564-9

AUTHORS

Akhil Sariki received his bachelor's degree in Electronics and communication from Indian Institute of Information Technology, Design & Manufacturing, Kancheepuram, India in 2020 and master's degree in VLSI Design from Dr B R Ambedkar National Institute of Technology Jalandhar, India in 2023 and. His areas of interest are low power, very large-scale integration design, application specific integrated circuit design and Silicon on chip.
Corresponding Author E-mail: akhils.vl.21@nitj.ac.in

Gatram Manoj Venkata Sai received his bachelor's degree in Electronics and communication from Indian Institute of Information Technology, Design & Manufacturing, Kancheepuram, India in 2020 and master's degree in VLSI Design and Embedded Systems from National Institute of Technology Rourkela, India in 2023 and. His areas of interest are low power, very large-scale integration design, application specific integrated circuit design and Silicon on chip.
E-mail: 221ec2335@nitrkl.ac.in

Mamta Khosla received her bachelor's degree in Electronics & Communication from REC Kurukshetra, India, and master's degree in Electronics & Communication Engineering from GNEC Ludhiana, India and PhD degree in Electronics & Communication Engineering from Dr B R Ambedkar National Institute of Technology Jalandhar, India. She is currently working as an Associate Professor in the Department of Electronics and communication Engineering, Dr B R Ambedkar NIT, Jalandhar. Her areas of interest are Digital Systems Design, Soft Computing, Nano scale Semiconductor Devices.
E-mail: khoslam@nitj.ac.in

Balwinder Raj received his bachelor's degree in Electronics Engineering from Punjab Technical University Jalandhar, India in 2004 and master's degree in Microelectronics from Panjab University Chandigarh, India in 2006 and PhD degree in Microelectronics and VLSI Design from IIT Roorkee, India in 2010. His areas of interest are Microelectronics and VLSI Design: He is currently working as an Associate Professor in the Department

of Electronics and communication Engineering, Dr B.R Ambedkar National Institute of Technology Jalandhar. His areas of interest are Microelectronics and VLSI Design: Novel Semiconductor Devices, Classical/Non-Classical Nanoscale Devices Modeling, Ultra Low Power VLSI/ULSI Design and Technology, Nanoscale Memory Design, Digital VLSI Circuit Design, and Reconfigurable FPGA Implementation.
E-mail: rajb@nitj.ac.in